


E540

NM-A161 Rev0.1 Schematic

***Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P-GL/ N14M-GV2***

2012-12-05 Rev 0.1

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
			Camera
	XHCI 1	0	
		1	USB Port (Right Side)
	2	2	USB Port (Left Side)
	3	3	
	4	4	
		5	USB Port (Right Side)
		6	
		7	
		8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS sensor support part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV GC6 support part
NOGC6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
dau1@	Support dau1 channel panel function

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

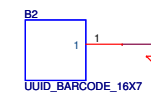
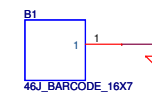
Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



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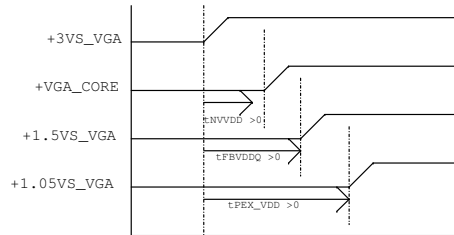
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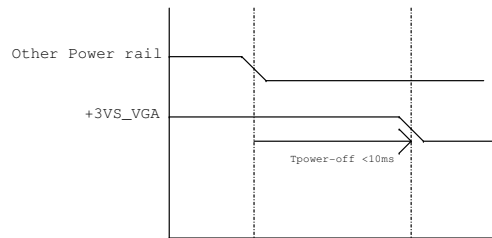
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus system VDB33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVD (1.8V)		I/O and PLLVD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

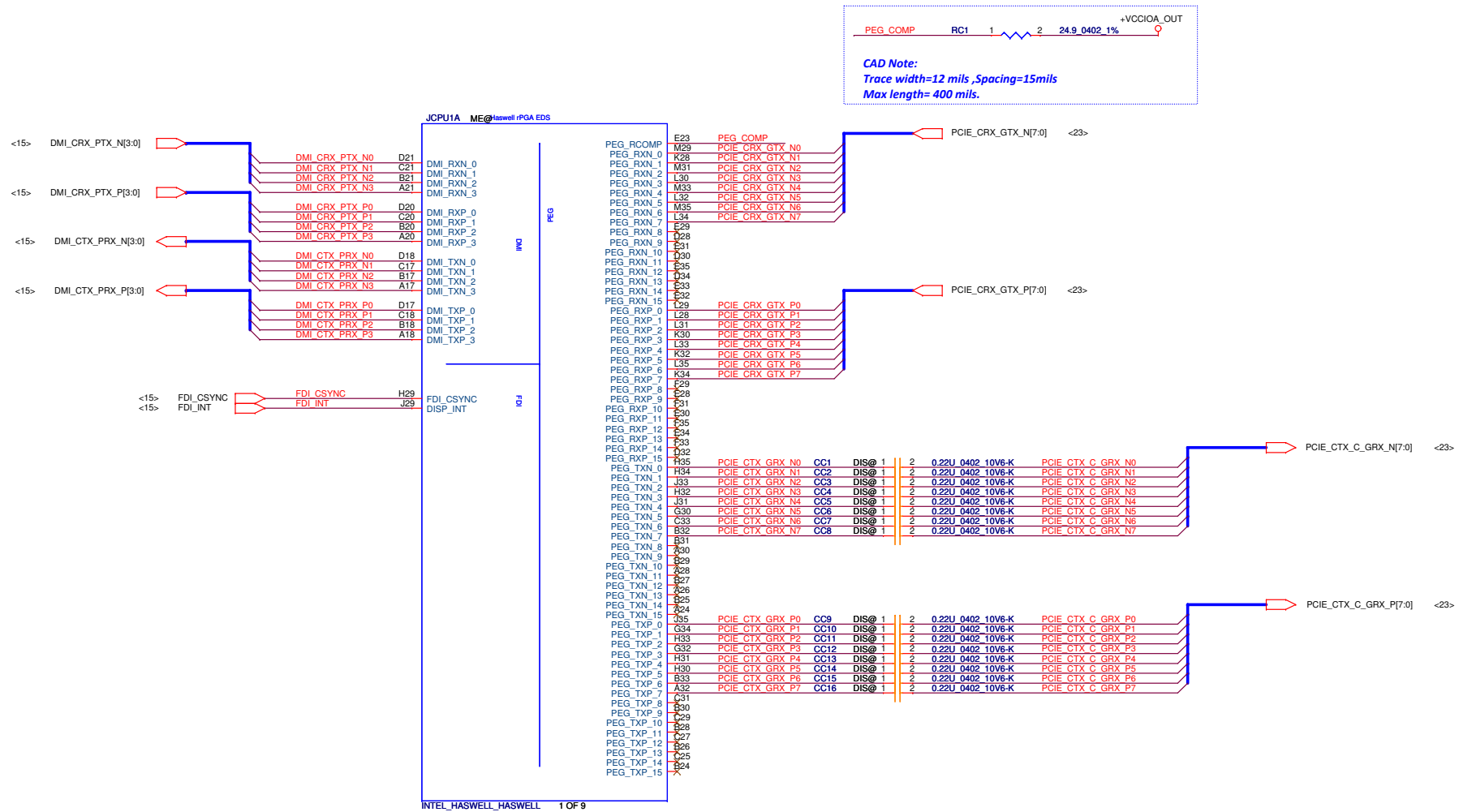
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

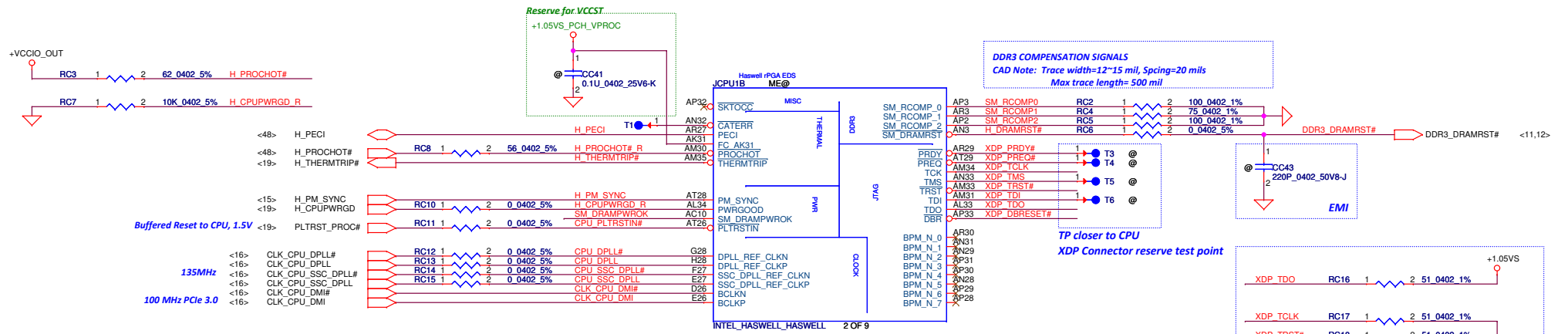
	Device ID		setting	I2C Slave addrees ID
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

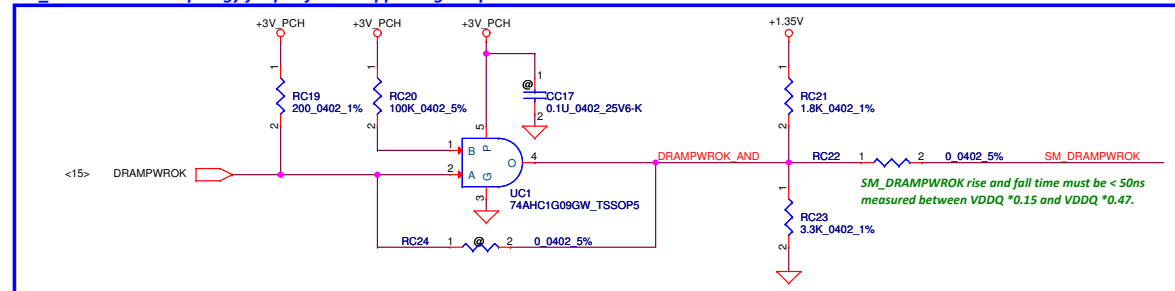
GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

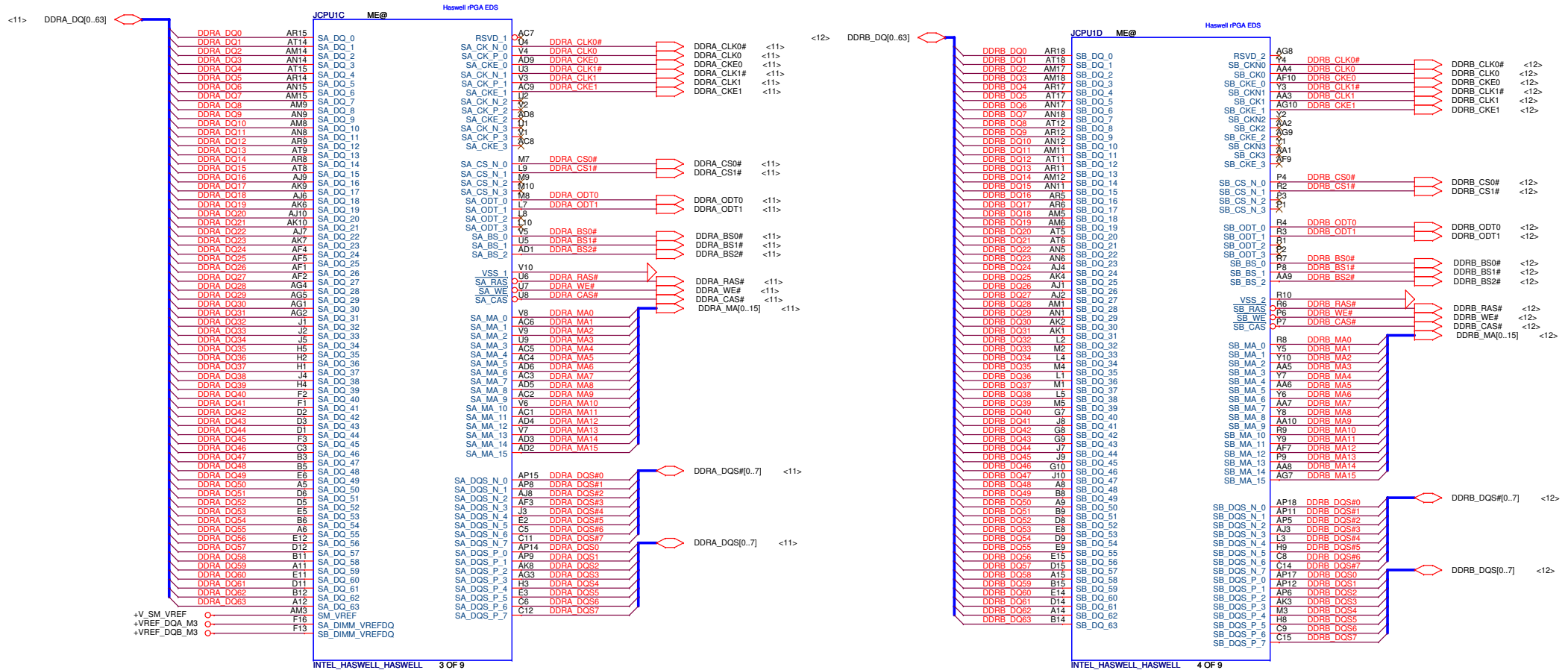
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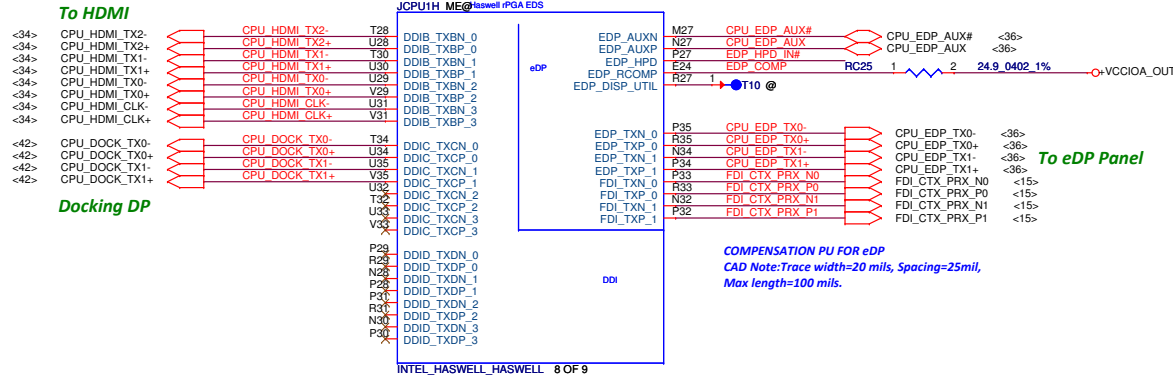




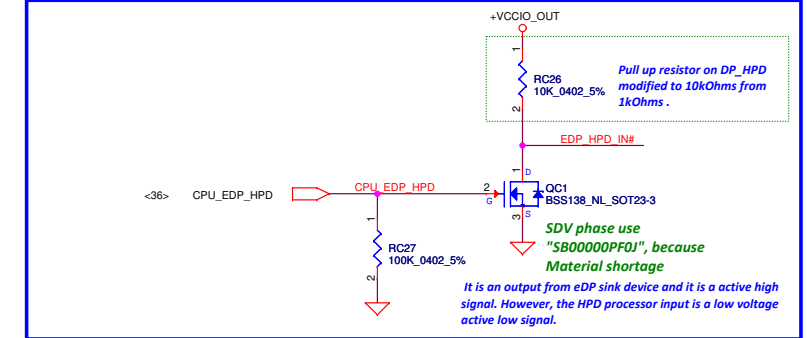
SM_DRAMPWROK Topology for platforms supporting Deep S3







HPD INVERSION FOR EDP



CFG STRAPS For CPU

(CFG[17:0] internal pull high 5~15K to VCCIO)

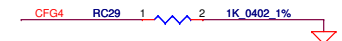
PEG Static Lane Reversal - CFG2 is for the 16x

- CFG2**
- 1: (Default) Normal Operation; Lane# definition matches socket pin map definition
 - 0: Lane Reversed



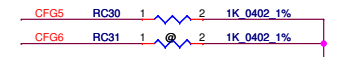
Display Port Presence Strap

- CFG4**
- 1: Disabled
 - No Physical Display Port attached to Embedded Display Port
 - 0: Enabled; An external Display Port device is connected to the Embedded Display Port



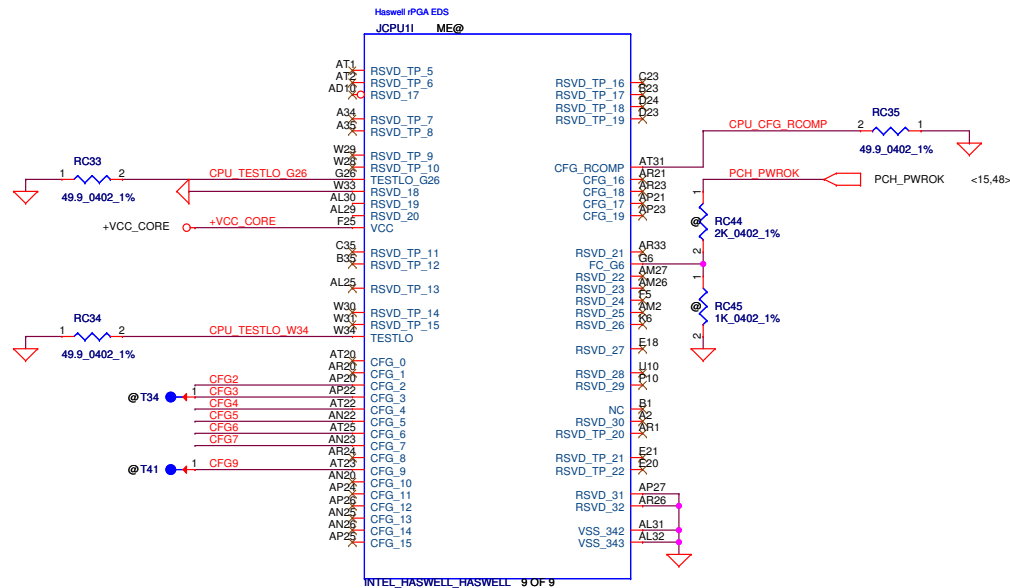
PCIe Port Bifurcation Straps

- CFG[6:5]**
- 11: Func 1 Disabled, Func 2 Disabled (x16,---,---)
 - 10: Func 1 Enabled, Func 2 Disabled (x8,x8,---)
 - 01: Func 1 Disabled, Func 2 Enabled
 - 00: Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

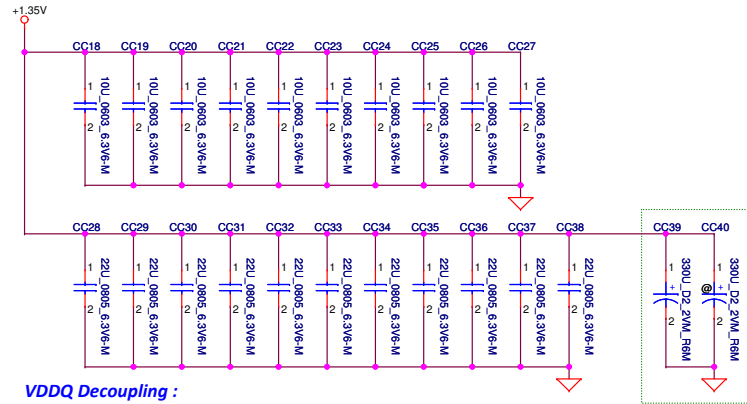


PEG DEFER TRAINING

- CFG7**
- 1: (Default) PEG Train Immediately Following XXRESETB Deassertion
 - 0: PEG Wait for BIOS for Training



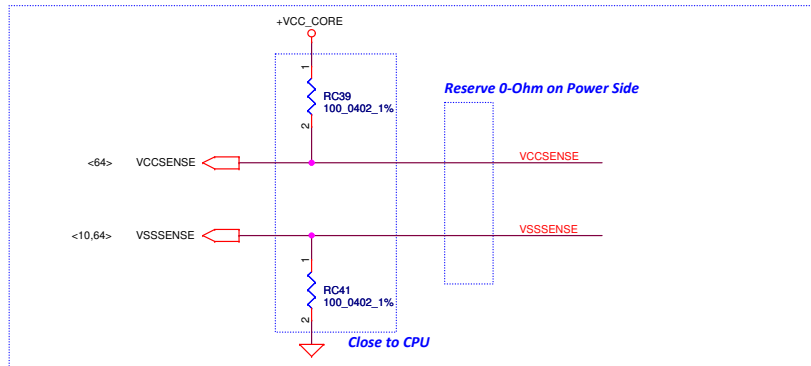
CPU VDDQ DECOUPLING



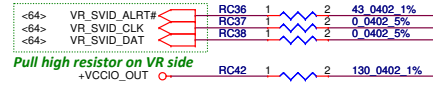
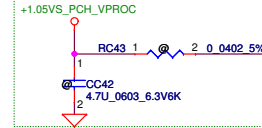
VDDQ Decoupling :

1. MB Bottom Socket Edge --> 2* 330uf, 6mΩ
2. 6x MB Bottom Socket Cavity --> 11* 22 μF (0805), 3mΩ
5x MB Top Socket Cavity
3. 5x MB Bottom Socket Cavity --> 10 x 10 μF (0805), 3mΩ
5x MB Top Socket Cavity

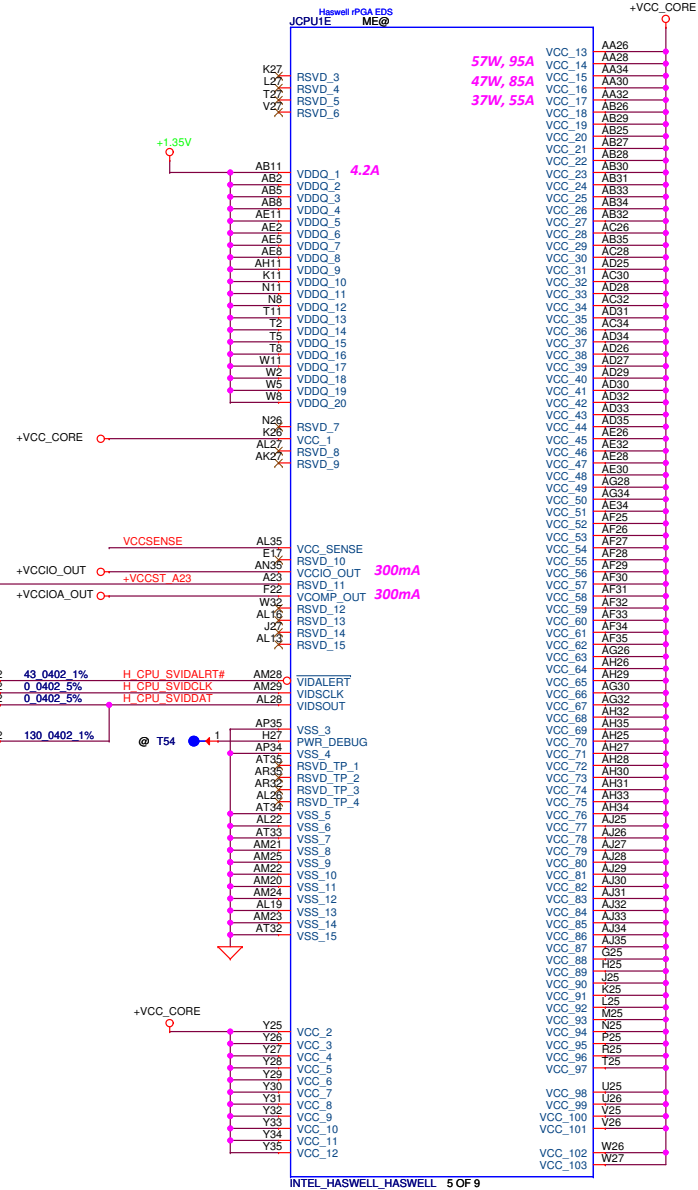
VCC/VSS SENSE

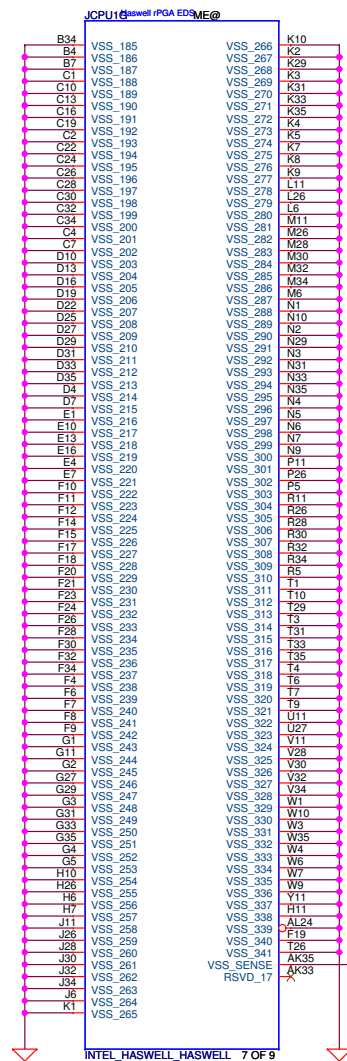
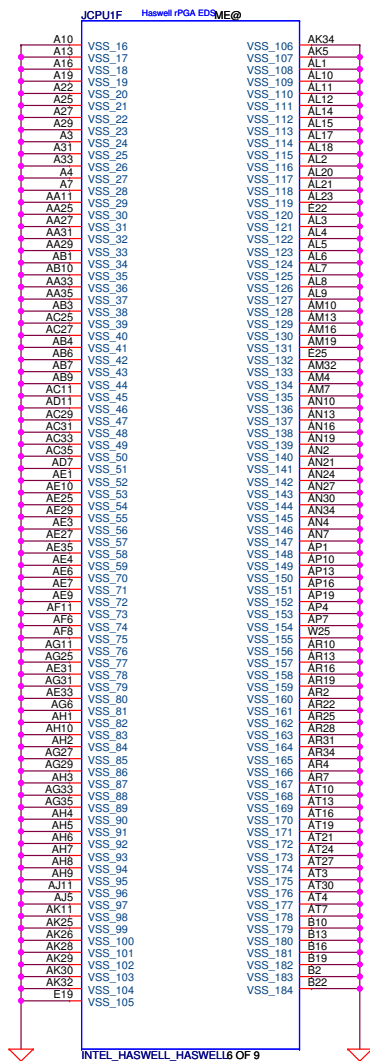


Reserve for VCCST



RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES



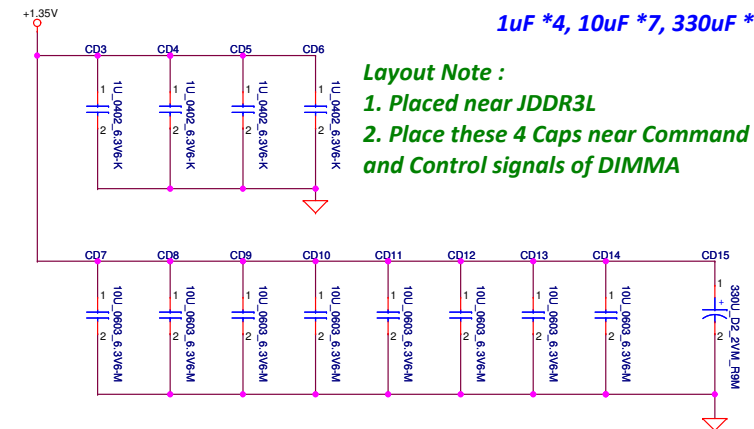


DDRA_DQ[0..63]	<7>
DDRA_DQS[0..7]	<7>
DDRA_DQS#[0..7]	<7>
DDRA_MA[0..15]	<7>

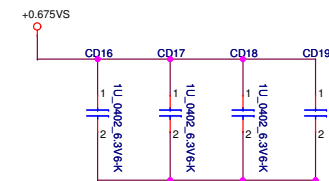



Layout Note :

1. Placed near JDDR3L
2. Place these 4 Caps near Command and Control signals of DIMMA

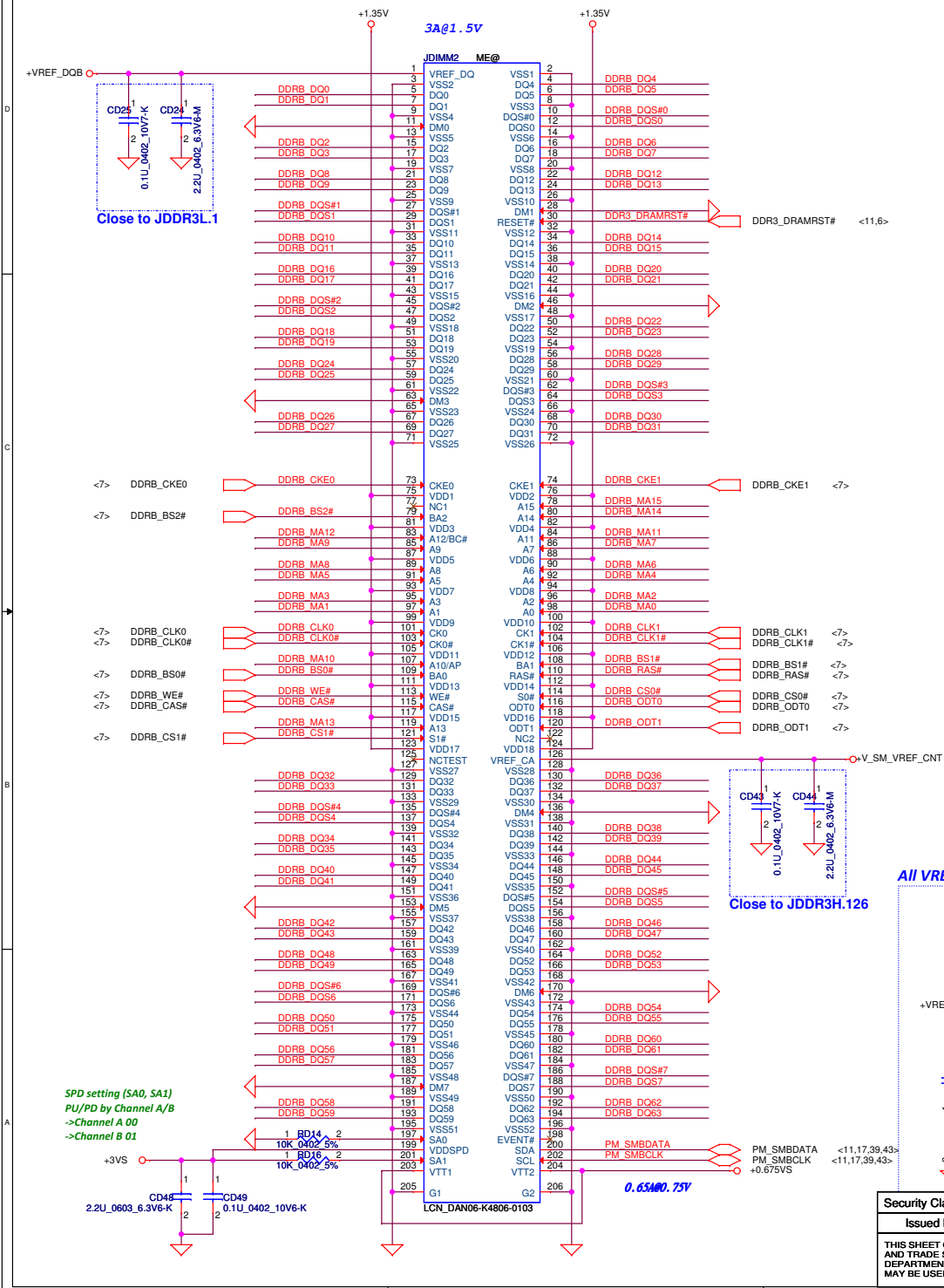


Layout Note : Placed near JDDR3L1.Pin203, 204

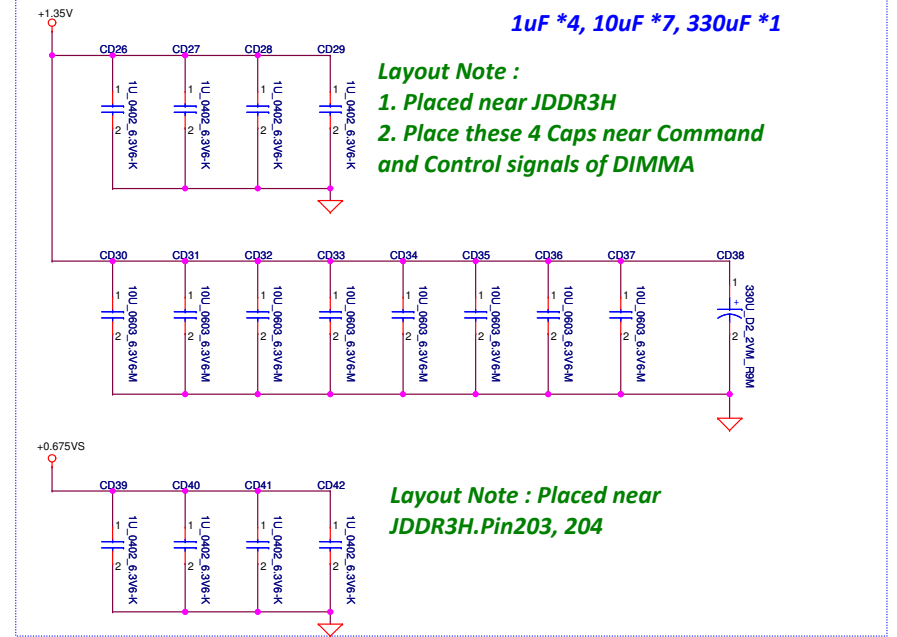


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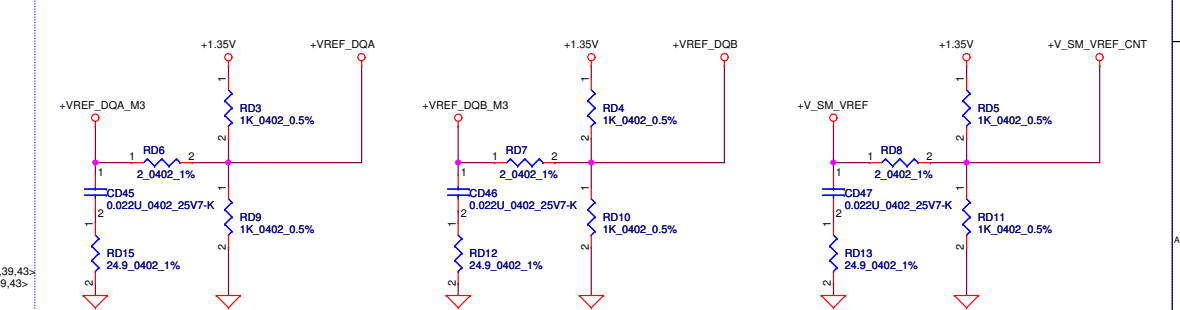
DDR3 SO-DIMM B



DDR Decoupling

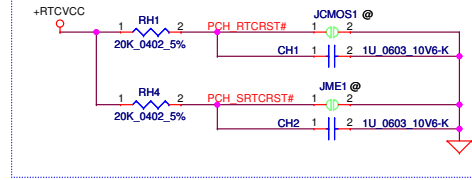


All VREF traces should have 20 mil trace width

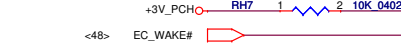
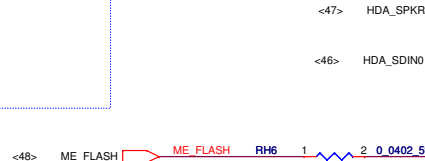
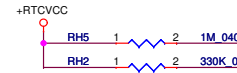
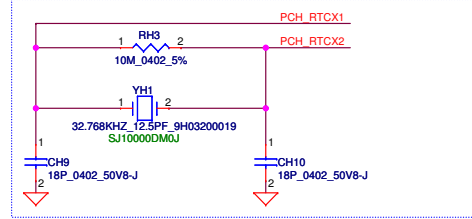


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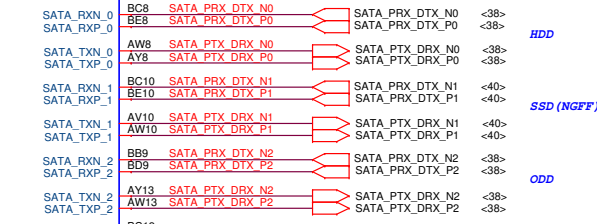
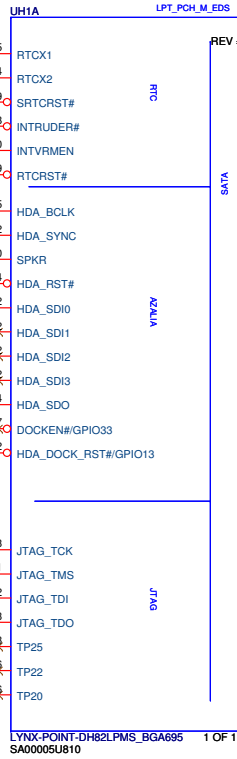
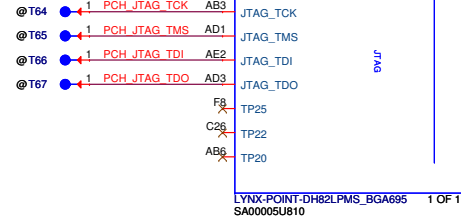
JCMOS, JME Setting, Need Under DDR Door



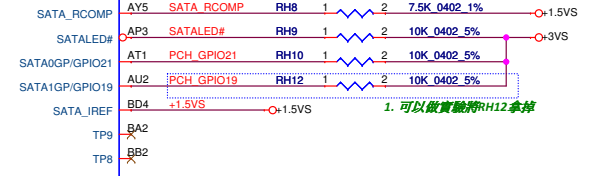
1. INTVRMEN, should always be pull high
★ H : Integrated VRM enable (Default)
L : Integrated VRM disable
2. Internal Voltage Regulator Enable:
This signal enables the internal 1.05 V regulators.



- During Reset", Immediately after Reset and S3/S4/S5
1. JTAG_TDI, JTAG_TMS --> Int. PU 20K
 2. JTAG_TCK --> Int. PD 20K
 3. JTAG_TDO --> High-Z

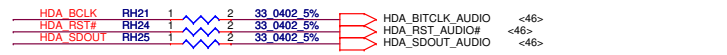


SATA Impedance Compensation :
--> Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

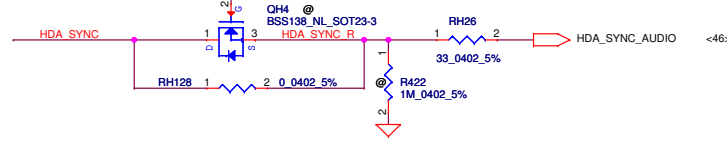


HDA AUDIO SIGNAL

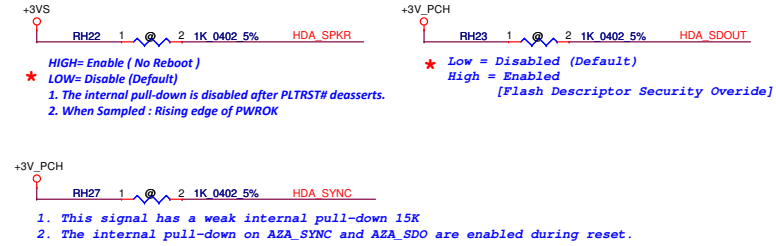
HDA AUDIO For Codec



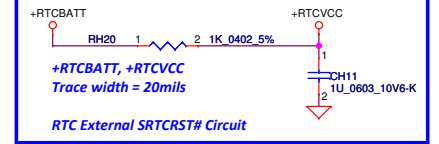
Isolation



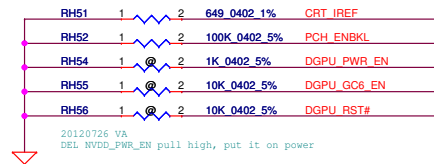
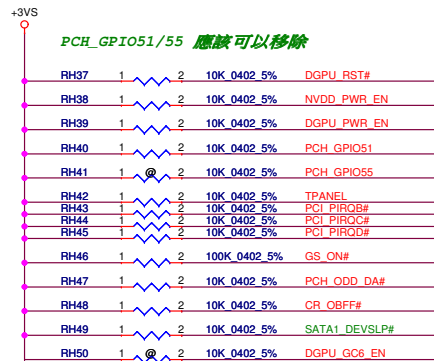
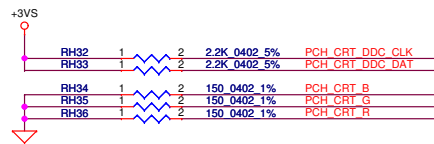
HDA STRAP



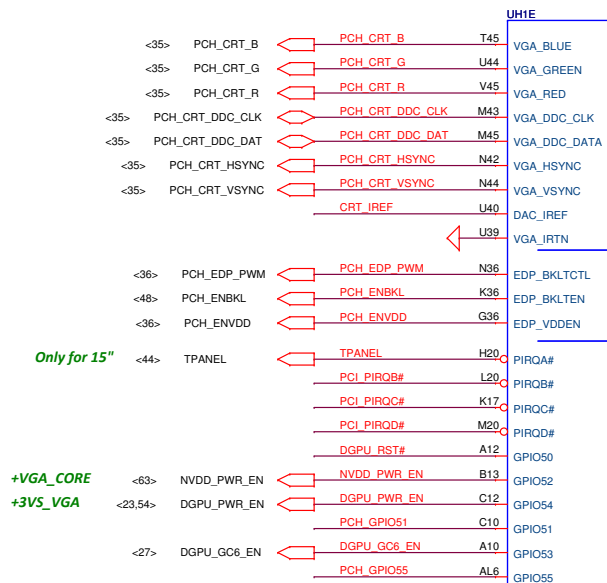
RTCVCC Circuit



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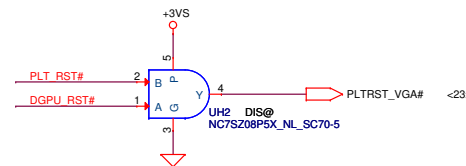


20120726 VA
DEL NVDD_PWR_EN pull high, put it on power



Only for 15"

+VGA_CORE
+3V5_VGA



check netname for LT3

To JIMIN1.Pin38

Integrated Pull-Up 20K

A16 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT3#

Low = A16 swap
override/Top-Block
Swap Override enabled

★ **High=Default

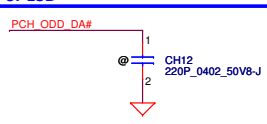
1. The signal has a weak internal pull-up, which is disabled after PLTRST# deasserts.
2. When sampled : Rising edge of PWROK

Boot BIOS Straps (BBS)

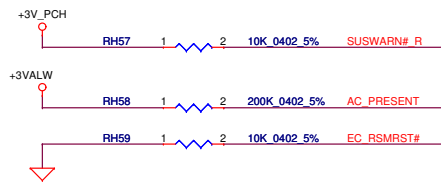
BBS_BIT1 (GPIO51)	BBS_BIT0 (GPIO19)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI ★

1. GPIO51/19 has weak internal pull-up via 20kohm
2. The internal pull-up is disabled after PLTRST# deasserts.
3. GPIO51 (bit 11) at the rising edge of PWROK
SATA1GP/GPIO19 (bit 10) at the rising edge of PWROK.

For ESD

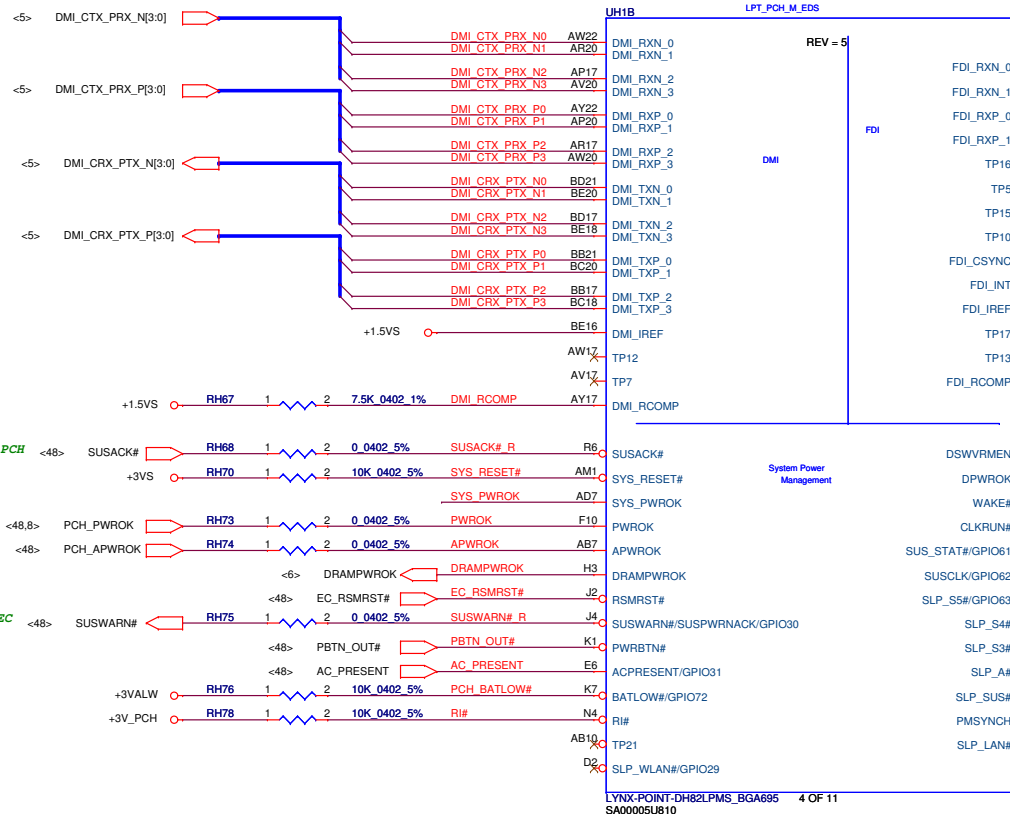
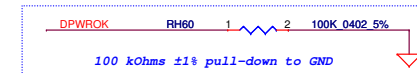
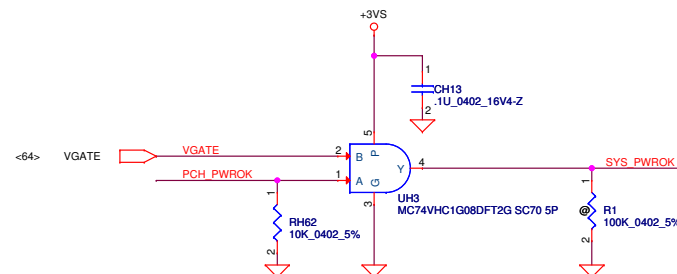


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Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size	Custom
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			Date	Monday, March 18, 2013	Sheet 14 of 57



SUSACK# R RH61 1 2 0 0402 5% SUSWARN# R

Stuff RH289 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit



EC to PCH <48> SUSACK# RH68 1 2 0 0402 5% SUSACK# R

+3VS RH70 1 2 10K 0402 5% SYS_RESET#

APWROK may come up earlier than PWRROK but no later

PCH_PWROK RH73 1 2 0 0402 5% PWRROK

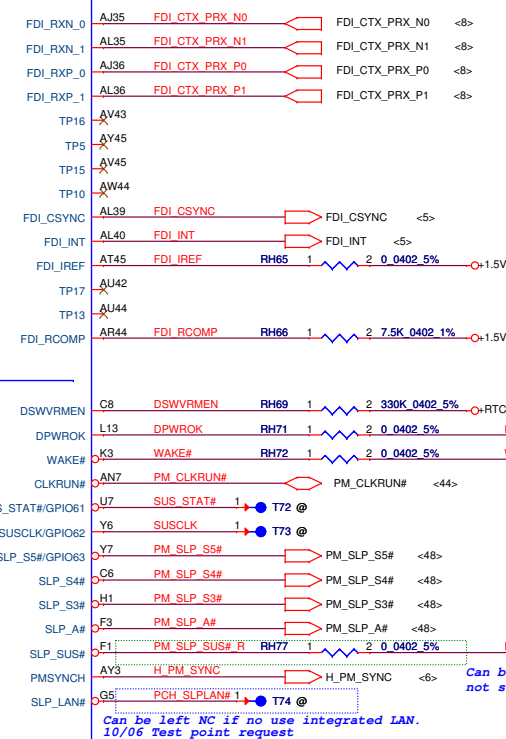
PCH_APWROK RH74 1 2 0 0402 5% APWROK

PCH to EC <48> SUSWARN# RH75 1 2 0 0402 5% SUSWARN# R

+3VALW RH76 1 2 10K 0402 5% PCH_BATLOW#

+3V_PCH RH78 1 2 10K 0402 5% RI#

APWROK only for A phase



DSWVRMEN must be always pulled high to +RTCVCC

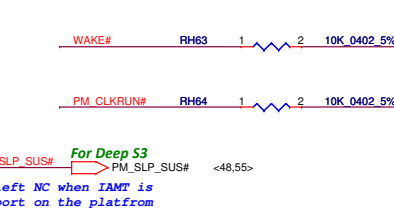
DSWVRMEN - Internal Deep Sleep 1.05V regulator

***H 'Enable

L 'Disable

For Deep S3

For LAN WAKE#



SUSCLK/GPIO62

This signal has a weak internal pull-up.

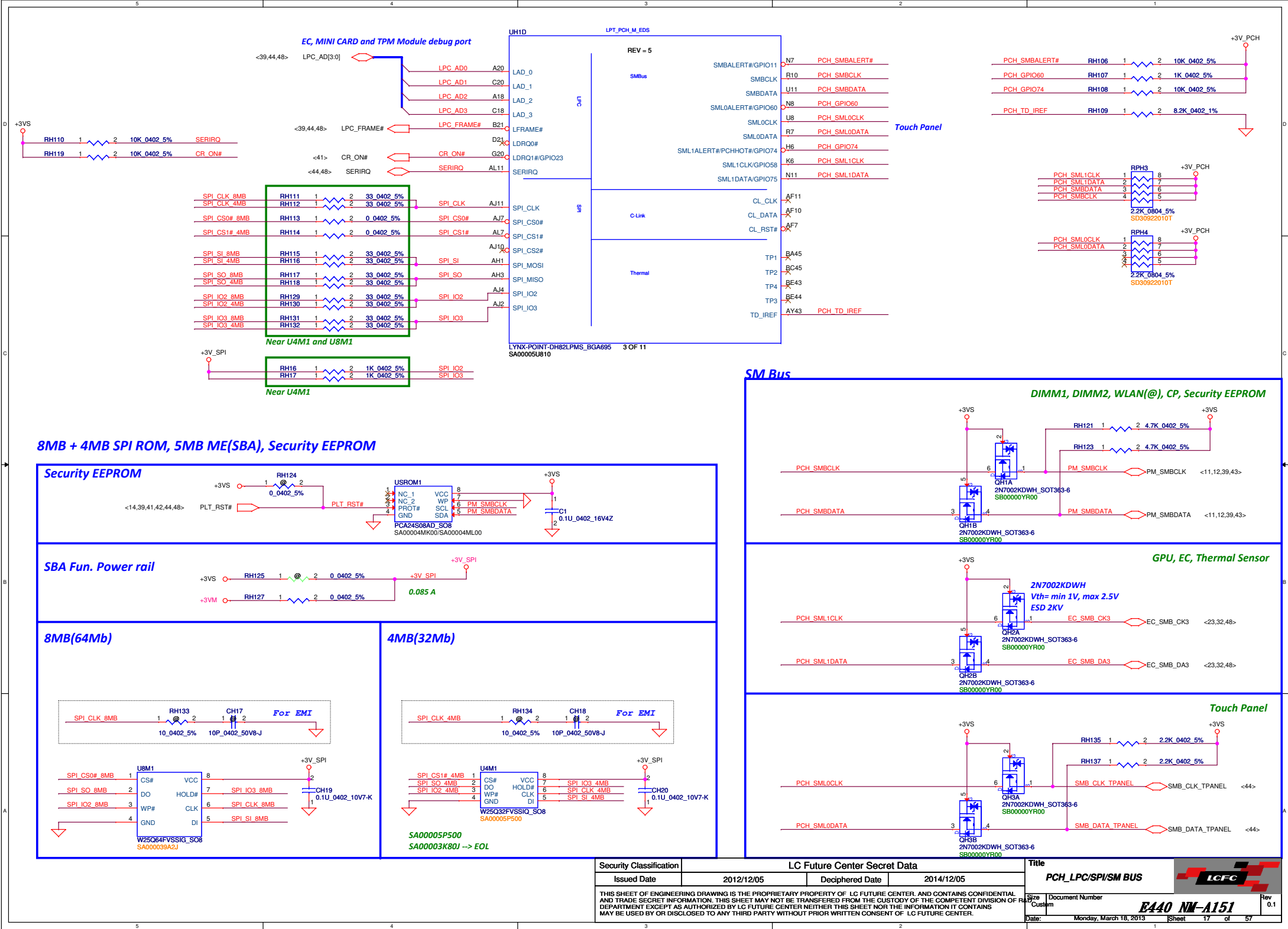
0 = Disable PLL On-Die voltage regulator.

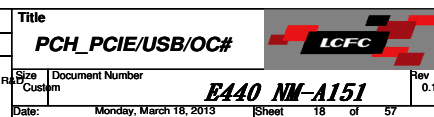
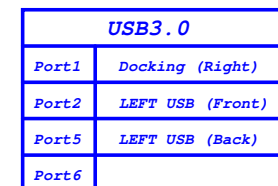
* 1 = Enable PLL On-Die voltage regulator.

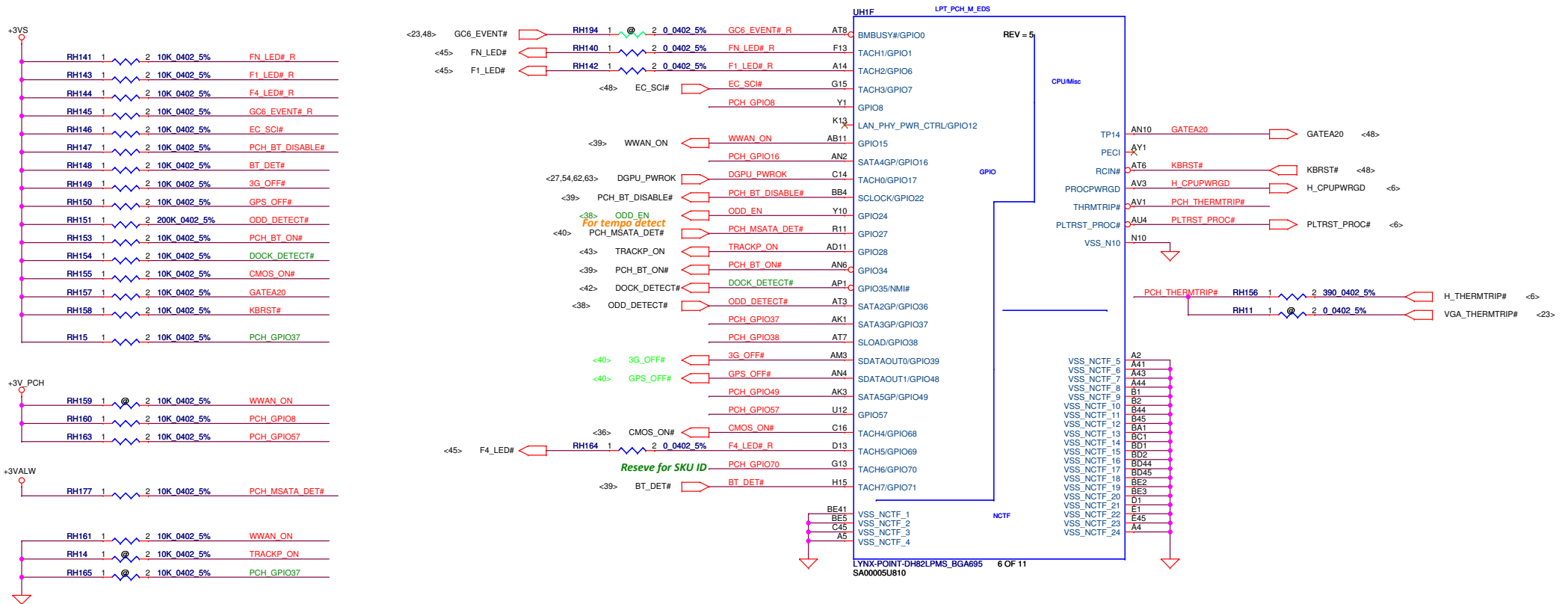
NOTES:

1. The internal pull-up is disabled after RSMRST# deasserts.

2. This signal is in the Suspend well.

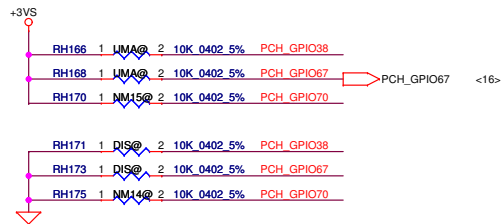




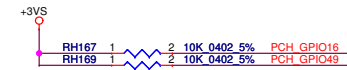


SKU ID

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1



CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01

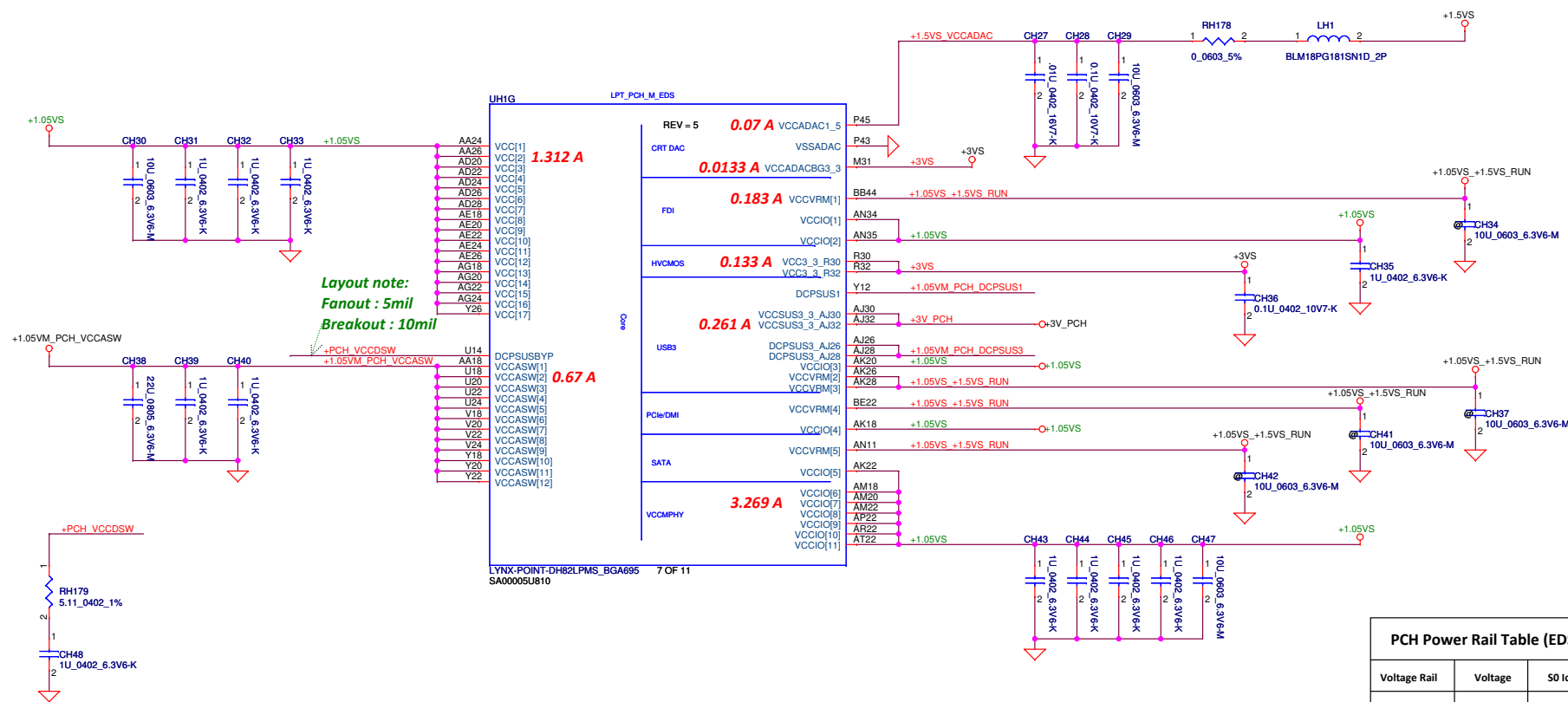


No use Flexible I/O pin, delete RH172, RH174

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3
				(00)	(00)							(00)	(00)				
				USB3 3	USB3 4							PCIE 1	PCIE 2				

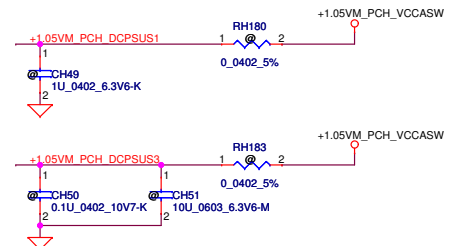
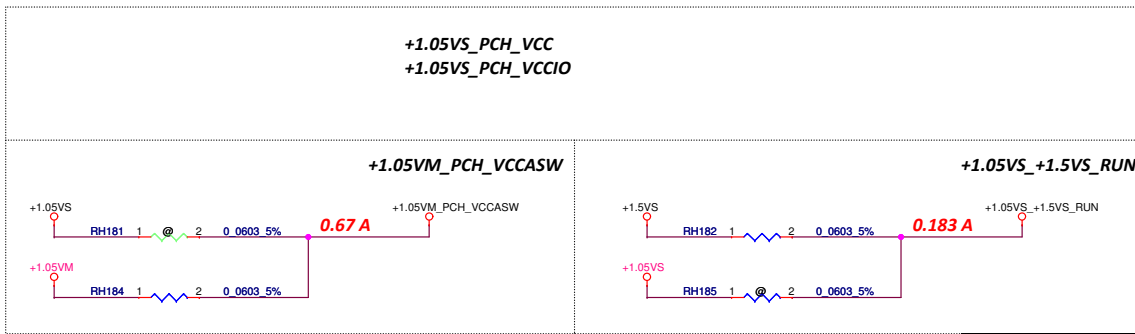
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Issued Date		2012/12/05		Deciphered Date		2014/12/05			
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						Size Custom		Document Number E440 NW-A151	
Date: Monday, March 18, 2013						Sheet 19 of 57			
						Rev 0.1			

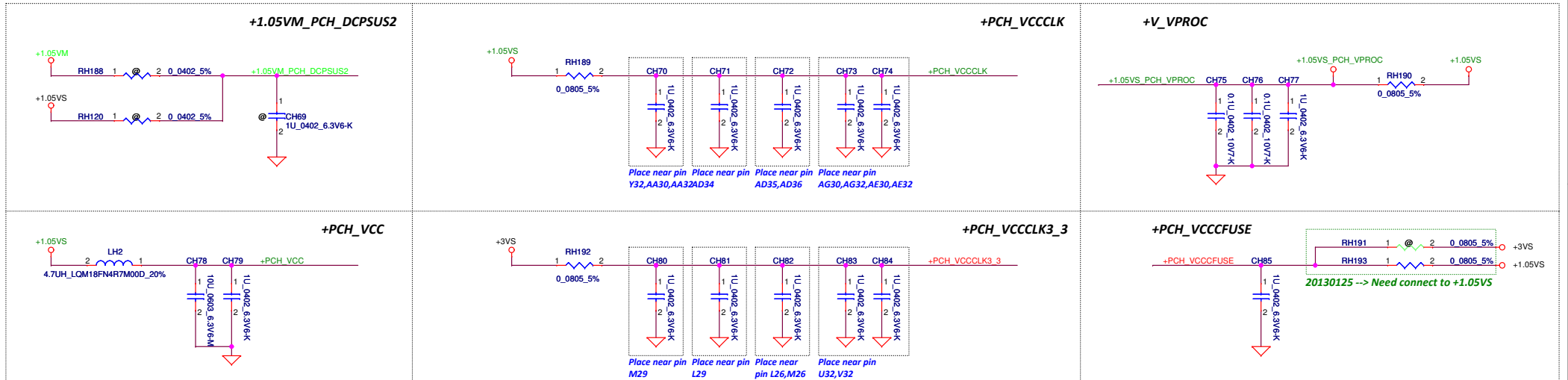
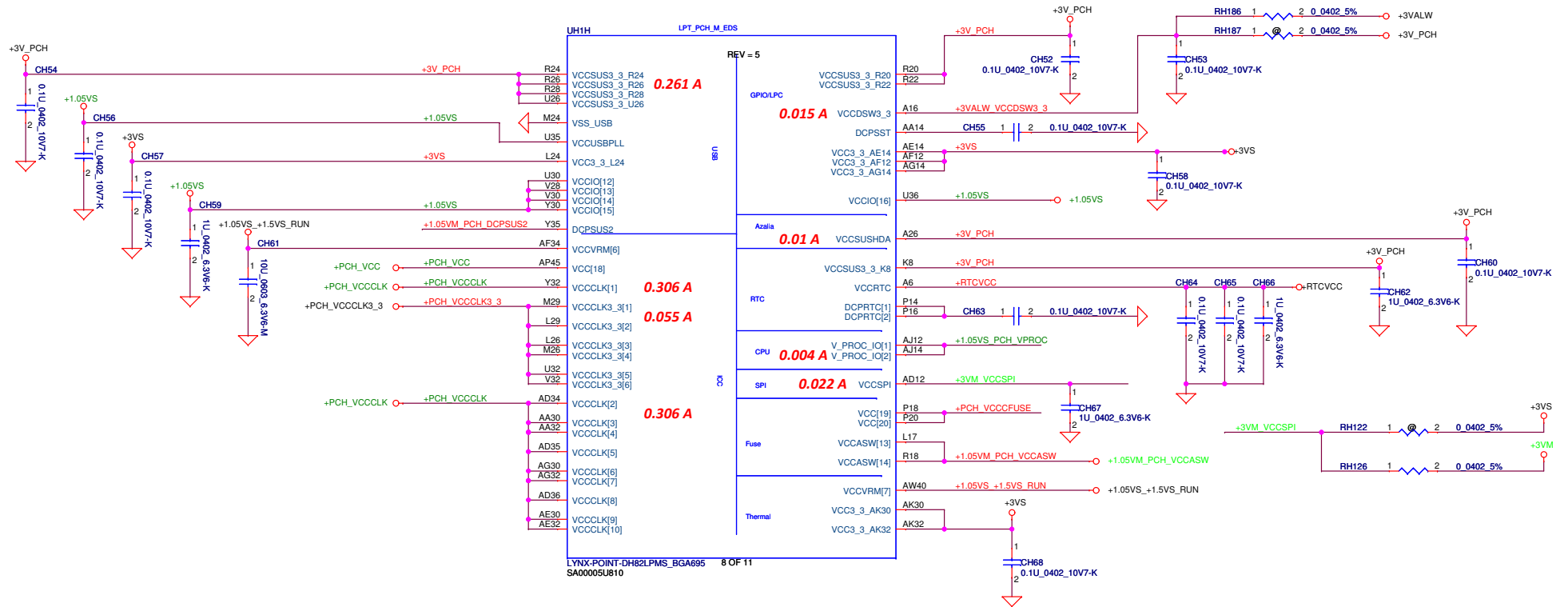
E440 NM-A151



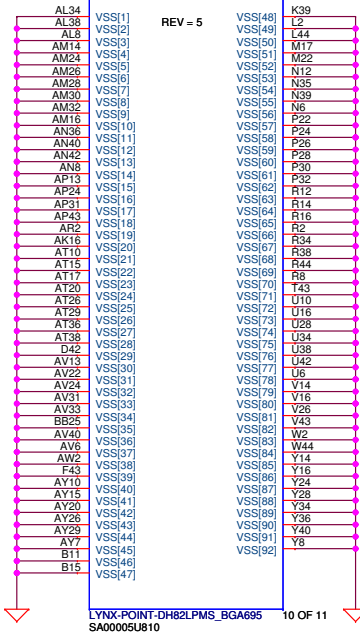
Layout note:
Fanout : 5mil
Breakout : 10mil

PCH Power Rail Table (EDS Rev1.0)		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.07 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

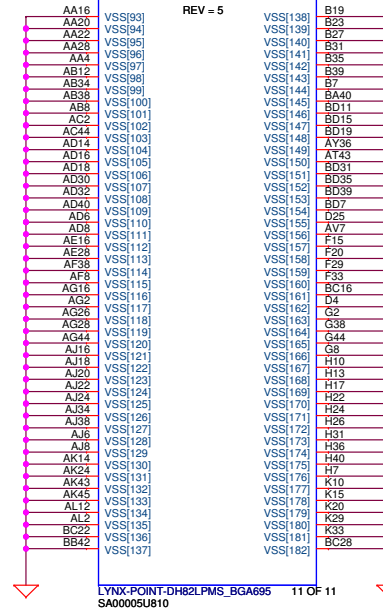


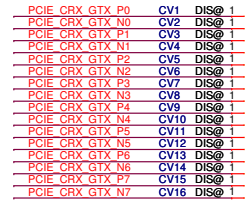


UH1J LPT_PCH_M_EDS



UH1K LPT_PCH_M_EDS





Security Classification

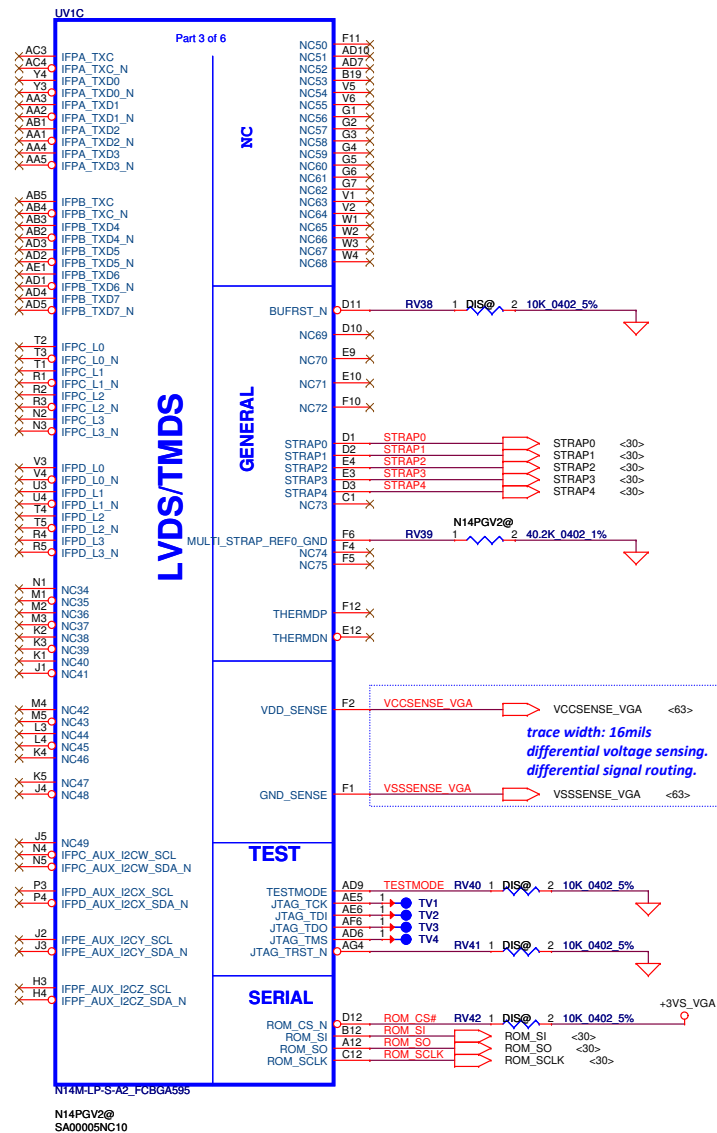
LC Future Center Secret Data

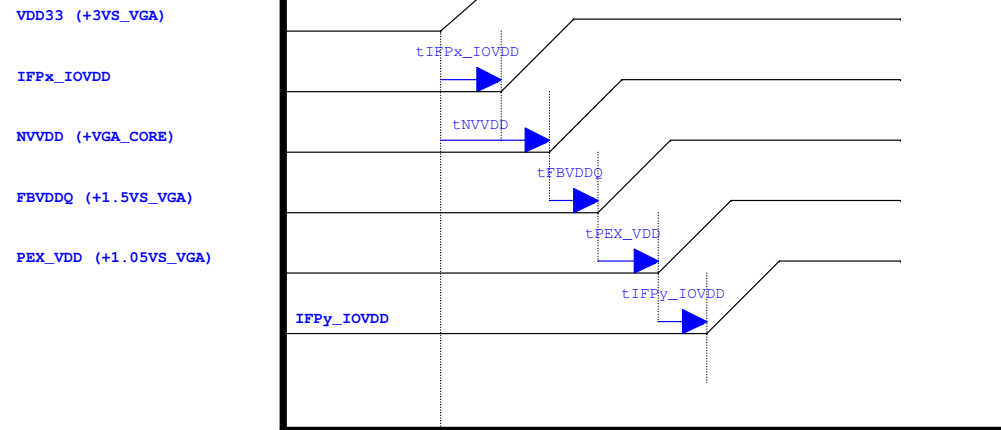
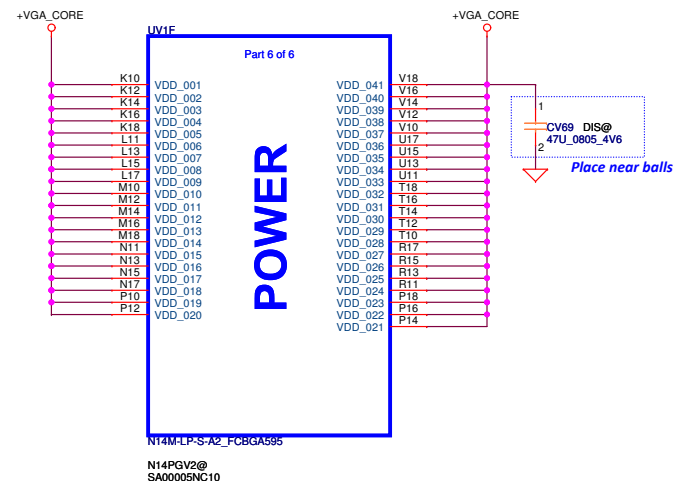
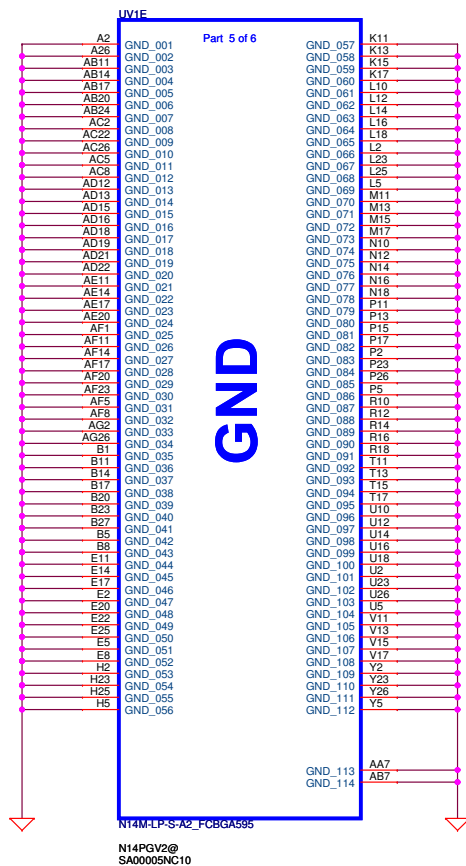
Title	
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N14P_PClc/GPIO/I2C [illegible]

Size Document Number Rev
F R&D Custom **E440 NM-A151** 0.1


Date:	Monday, March 18, 2013	Sheet	23	of	57
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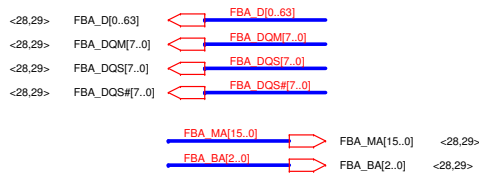




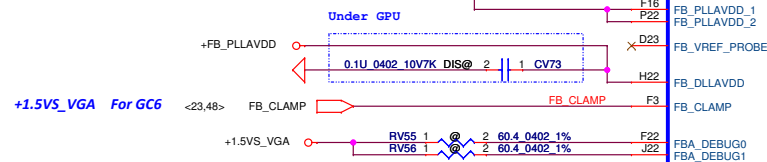
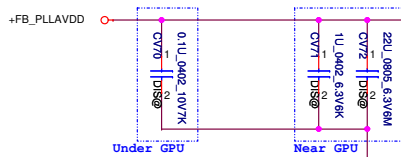
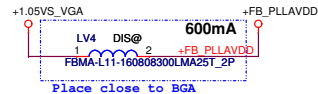
NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

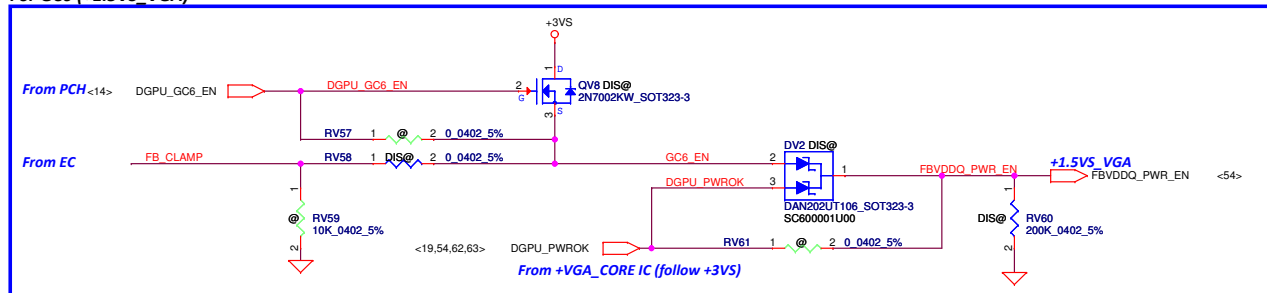
Security Classification	LC Future Center Secret Data			Title	N14P_VDD/GND	
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				E540 NM-A161		
				Date:	Monday, March 18, 2013	Sheet 26 of 57



30ohms (ESR=0.01) Bead
P/N: SM010007W00

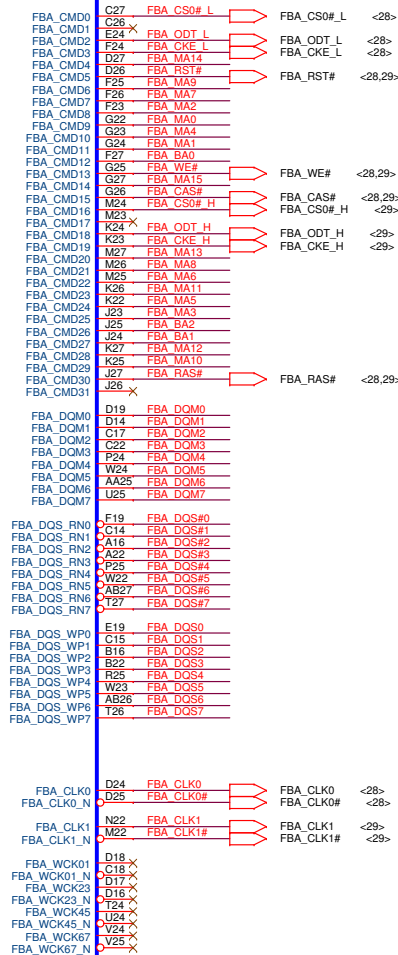


For GC6 (+1.5VS_VGA)



Part 2 of 6

MEMORY
INTERFACE A



Mode D - Mirror Mode Mapping

Address	DATA Bus
FBx_CMD0	CS0#_L
FBx_CMD1	ODT_L
FBx_CMD2	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	ODT_H
FBx_CMD18	CKE_H
FBx_CMD19	A13 A13
FBx_CMD20	A8 A8
FBx_CMD21	A6 A6
FBx_CMD22	A11 A11
FBx_CMD23	A5 A5
FBx_CMD24	A3 A3
FBx_CMD25	BA2 BA2
FBx_CMD26	A12 A12
FBx_CMD27	A10 A10
FBx_CMD28	RAS# RAS#

Security Classification

LC Future Center Secret Data

Issued Date

2012/12/05

Deciphered Date

2014/12/05

Title

N14P_MEM IF/FB CLAMP

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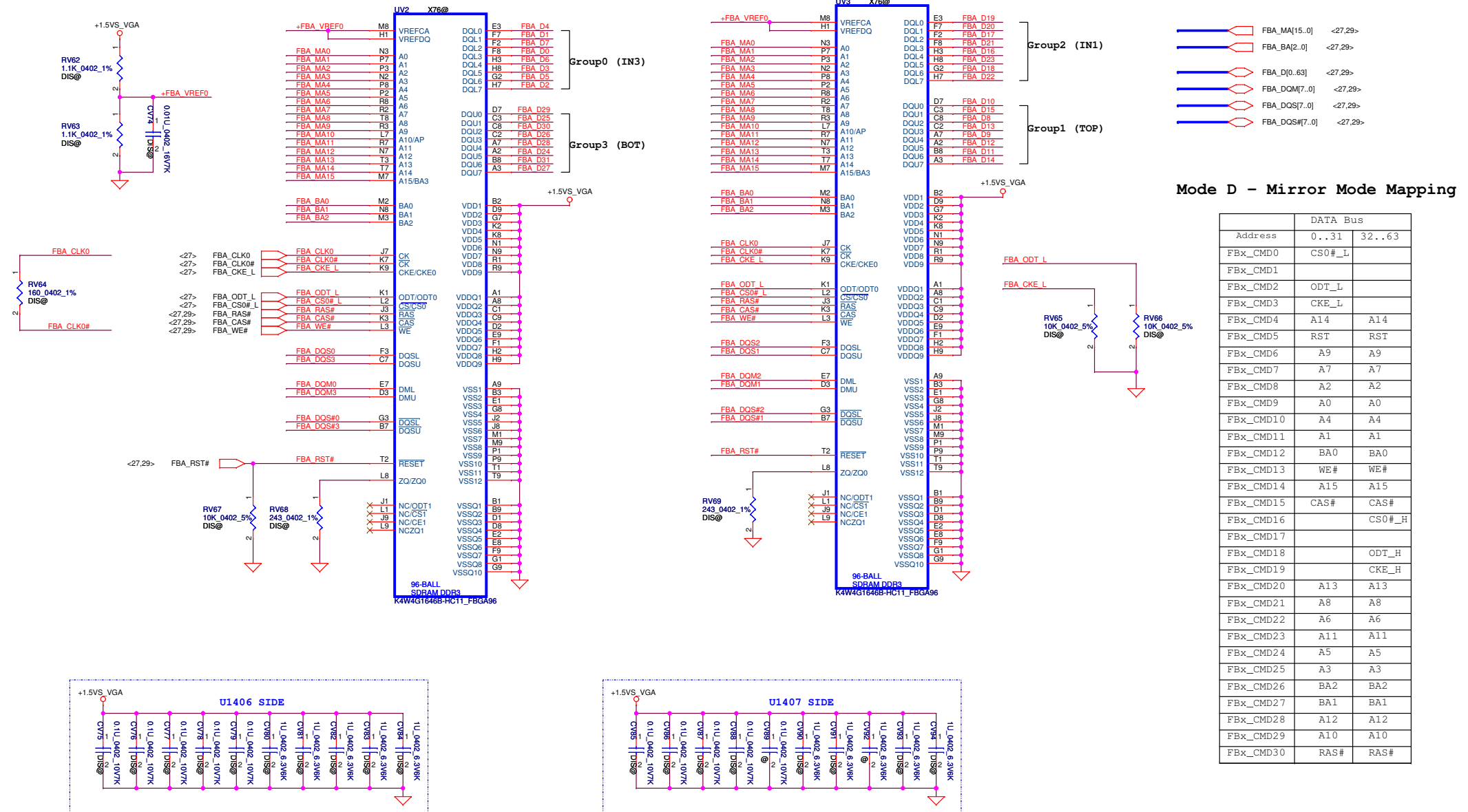
E440 NM-A151

Date: Monday, March 18, 2013

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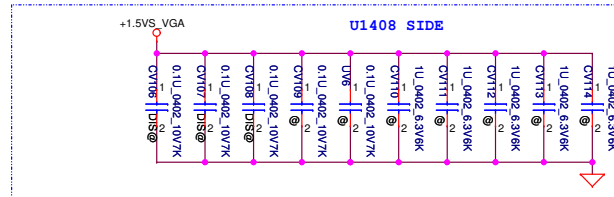
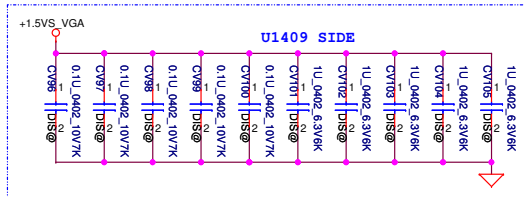
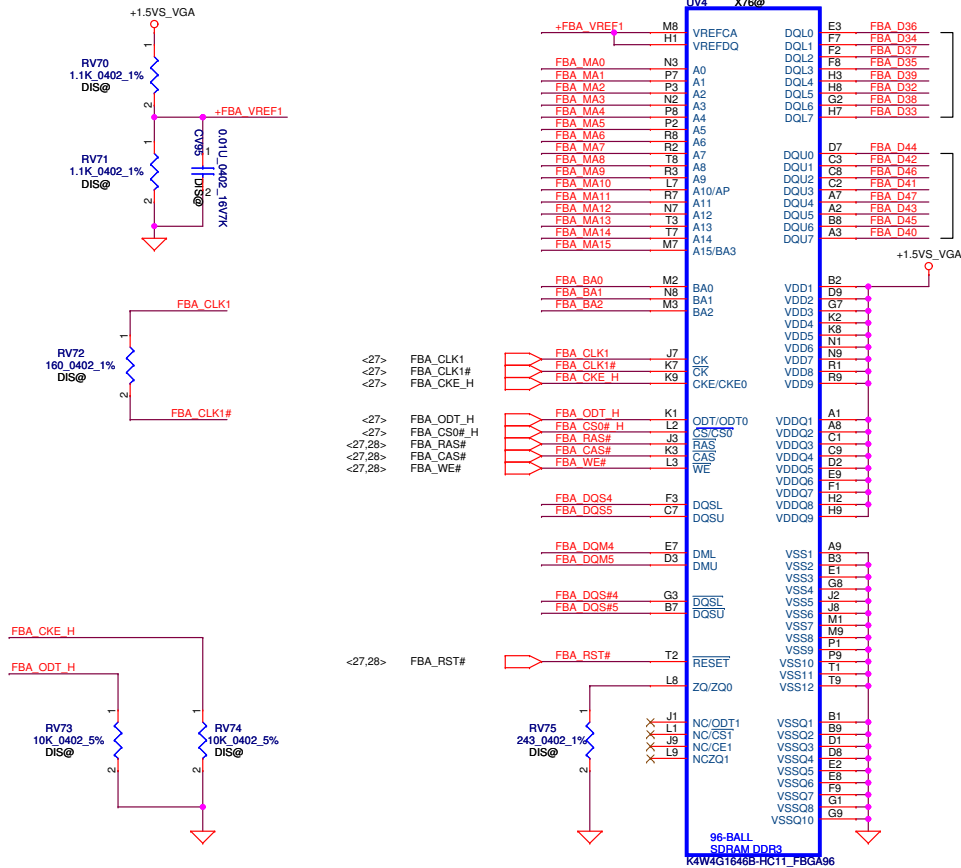
Rev 0.1

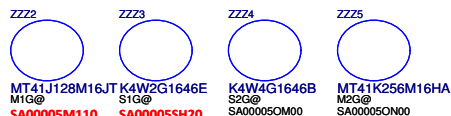
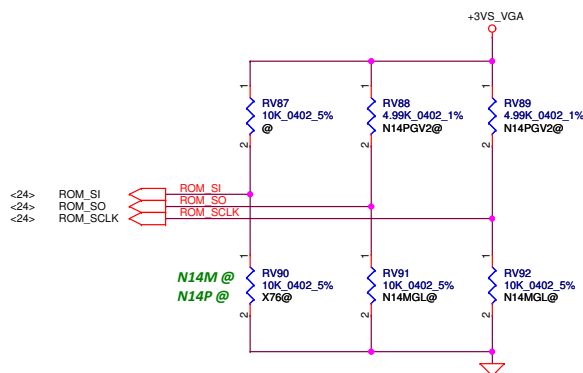
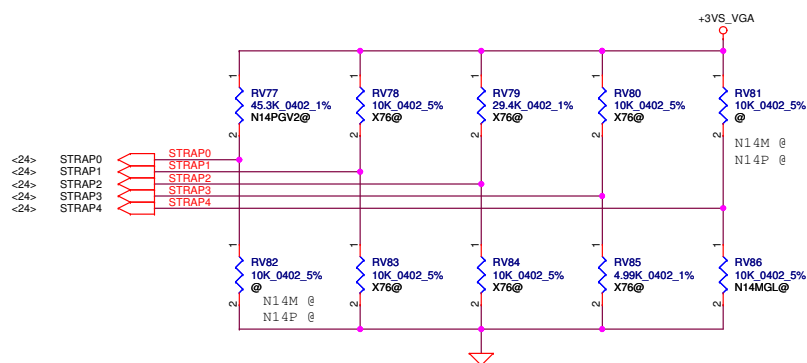
Memory Partition A - Lower 32 bits



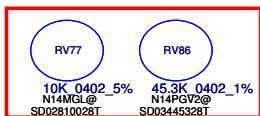
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition A - Upper 32 bits

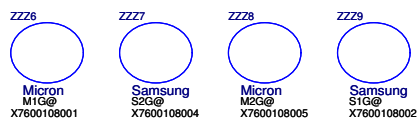




For N14P-GV2 QS Sample
ROM_SO change from PU 10K to PU 5K
ROM_SCLK change from PD 15K to PU 5K
STRAP1 change from PD 5K to PD 45K
STRAP2 change from PU 30K to PD 15K
STRAP4 change from PD 5K to PD 45K



Load BOM時，要改成RV86，RV77



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

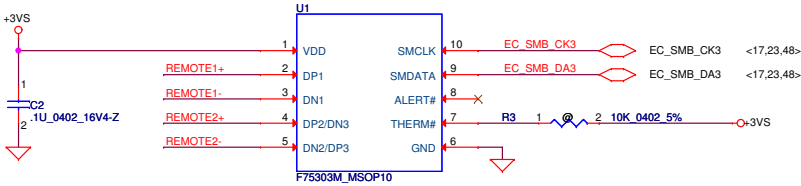
USER Straps	
User [3:0]	
1000-1100	Customer defined

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

DP_PLL_VDD33V	
0	Reserved
1	Default

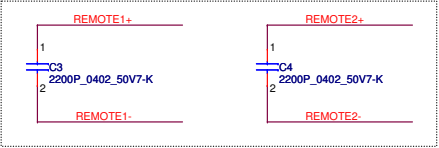
Thermal Sensor

Thermal Sensor
placed near by VRAM

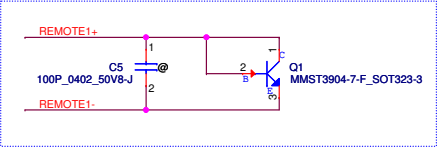


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

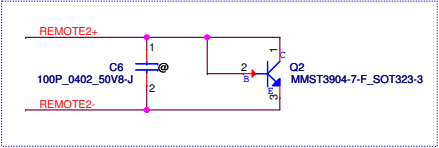
Close to U2



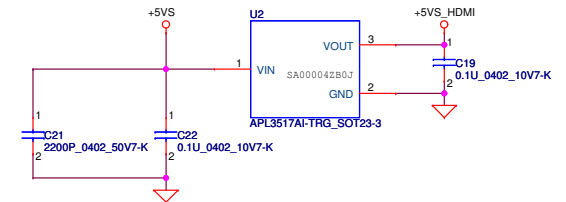
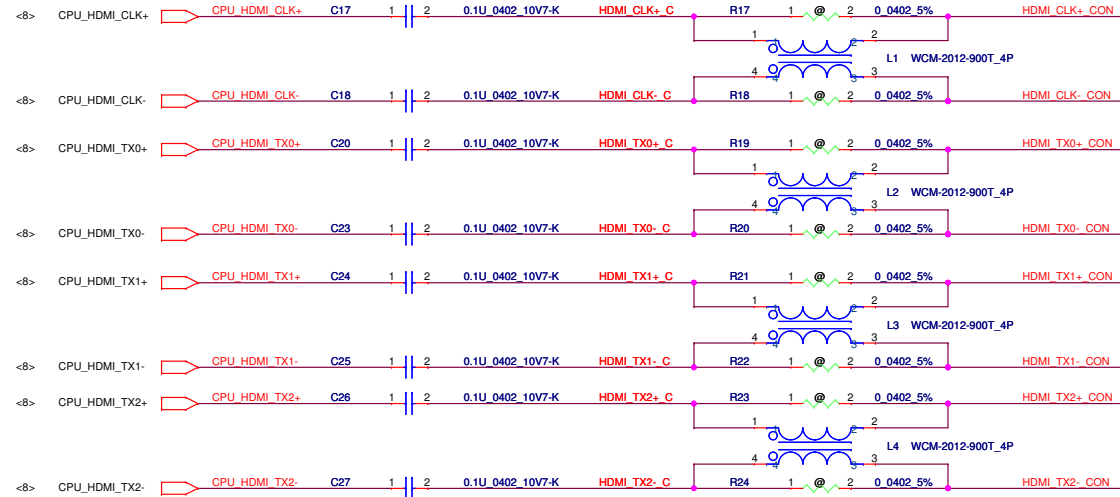
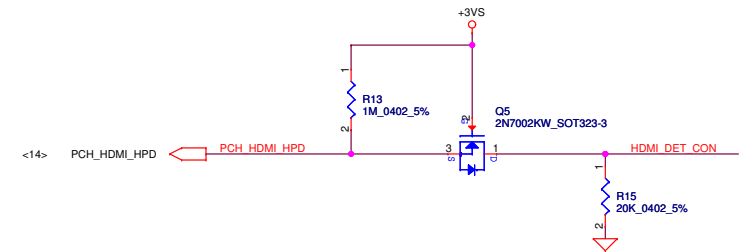
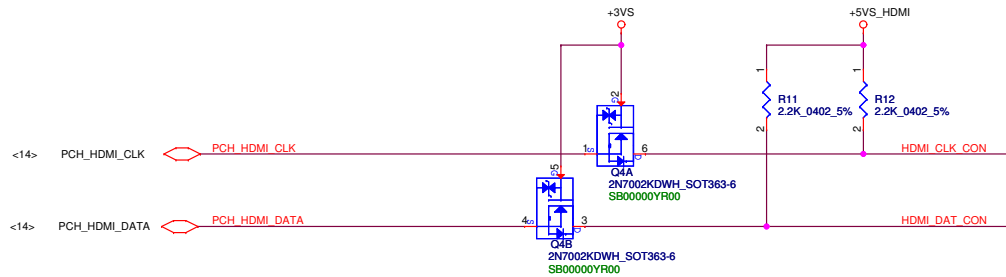
Close to BOTTOM DDR3



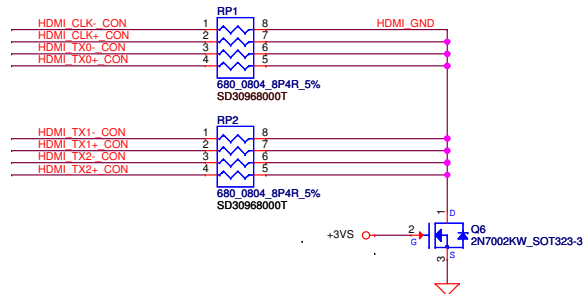
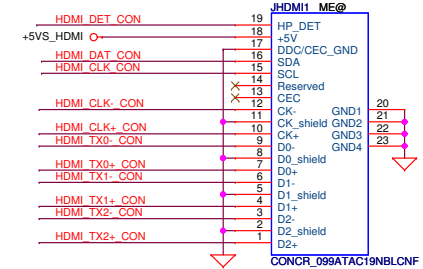
Close to +CPU_CORE



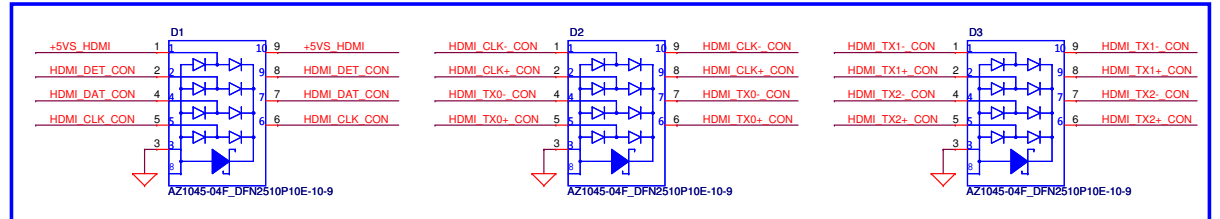
REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



HDMI CONN.



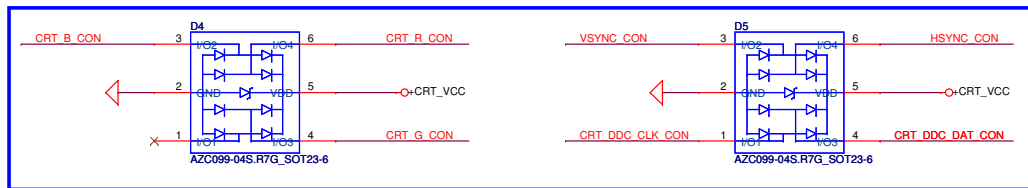
For ESD



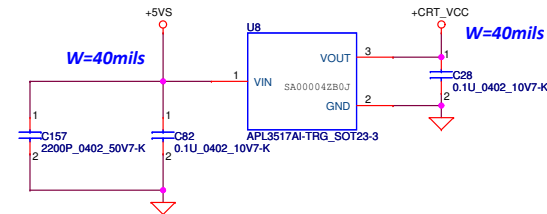
45@1
45@
HDMI+HDCP
R000000040J

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Issued Date	2012/12/05	Deciphered Date
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Title	Document Number	Rev
HDMI CONN.	E440 NM-A151	0.1
Date:	Monday, March 18, 2013	Sheet 34 of 57

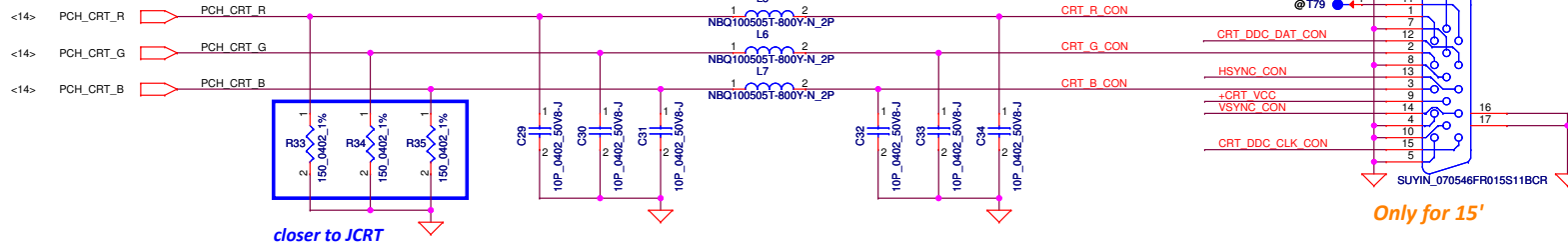


closer to JCRT



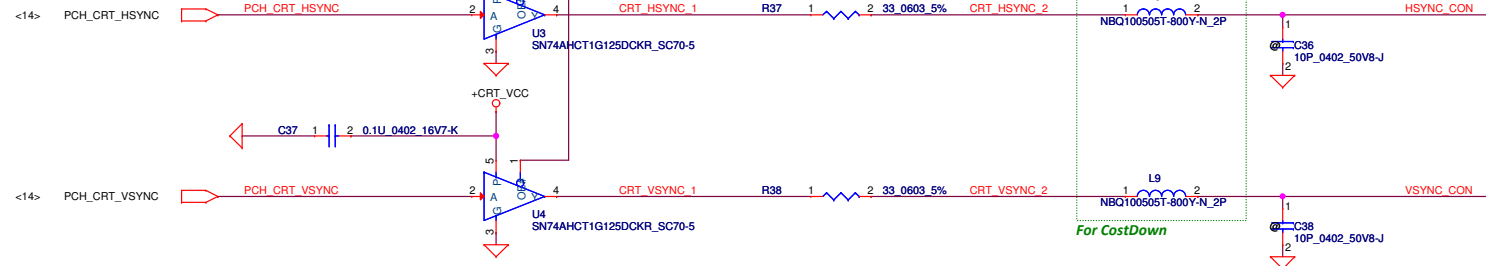
CRT Connector

From PCH

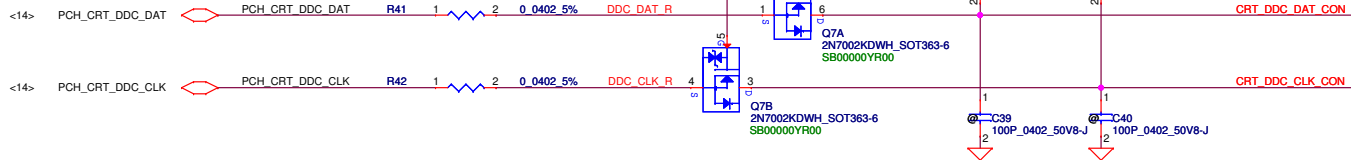



Only for 15'

From PCH

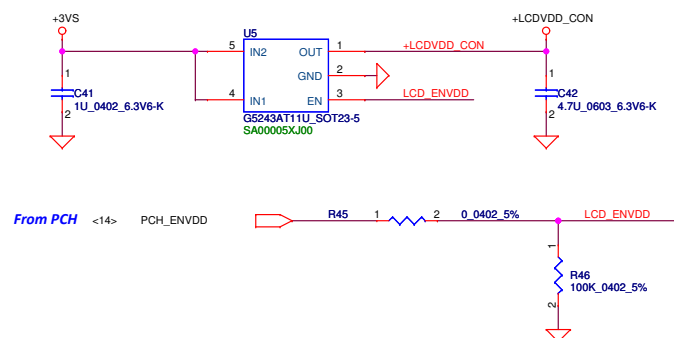


From PCH

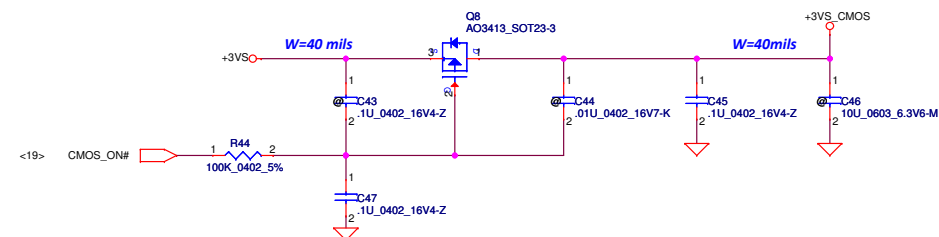


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Size		Document Number		E540 NW-A161		Rev
Custom		Monday, March 18, 2013		Sheet 35 of 57		0.

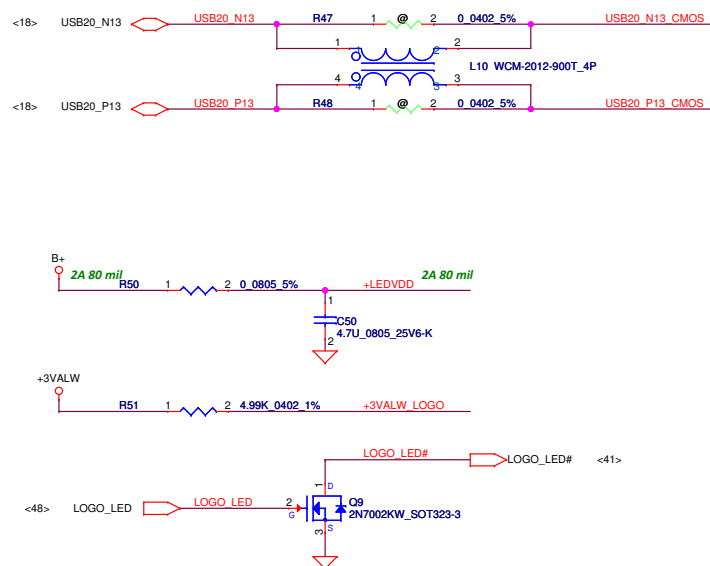
LCDVDD Circuit



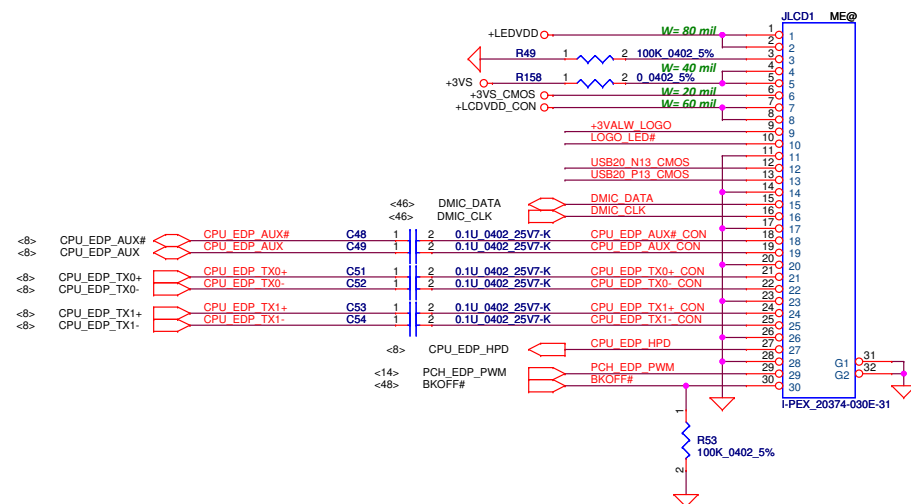
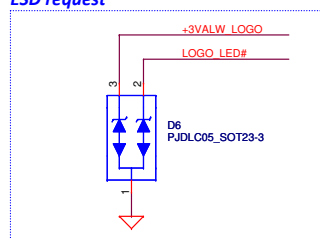
CMOS Camera




CMOS USB Port10

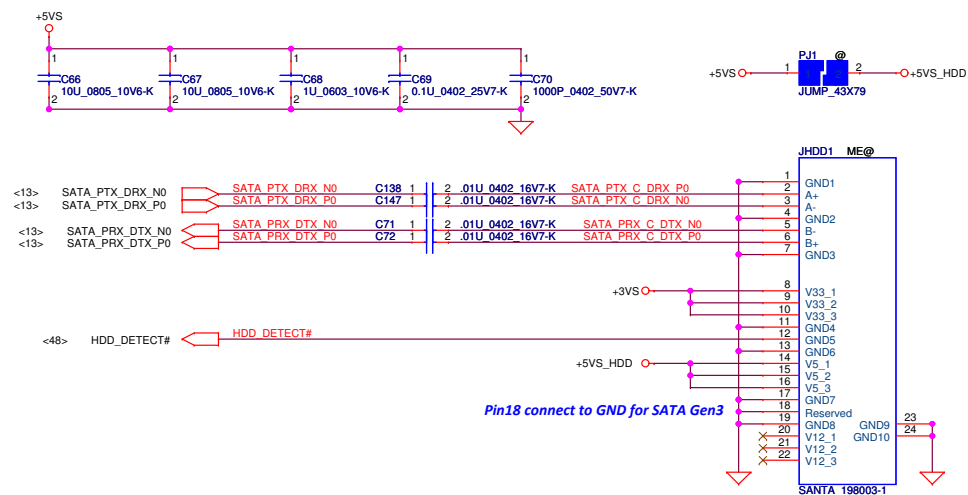


ESD request



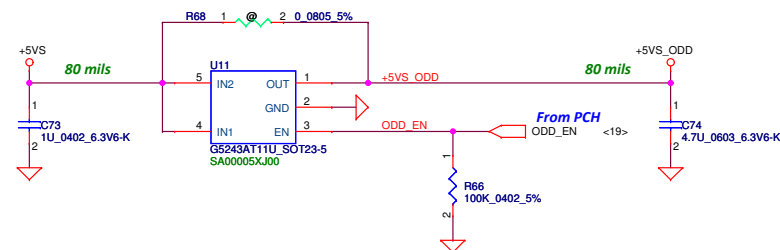
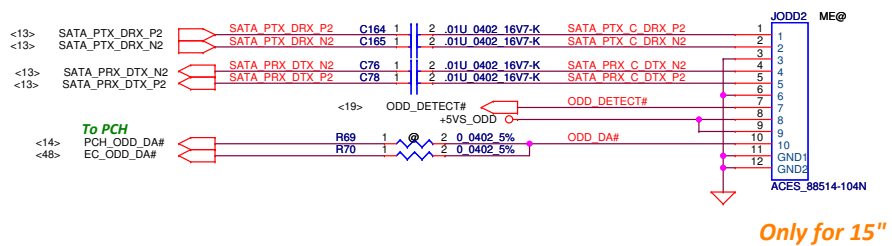
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2012/12/05	Deciphered Date	2014/12/05	LCD/CMOS CONN.			
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				Date:	Monday, March 18, 2013	Sheet 36 of 57	

SATA HDD CONN.

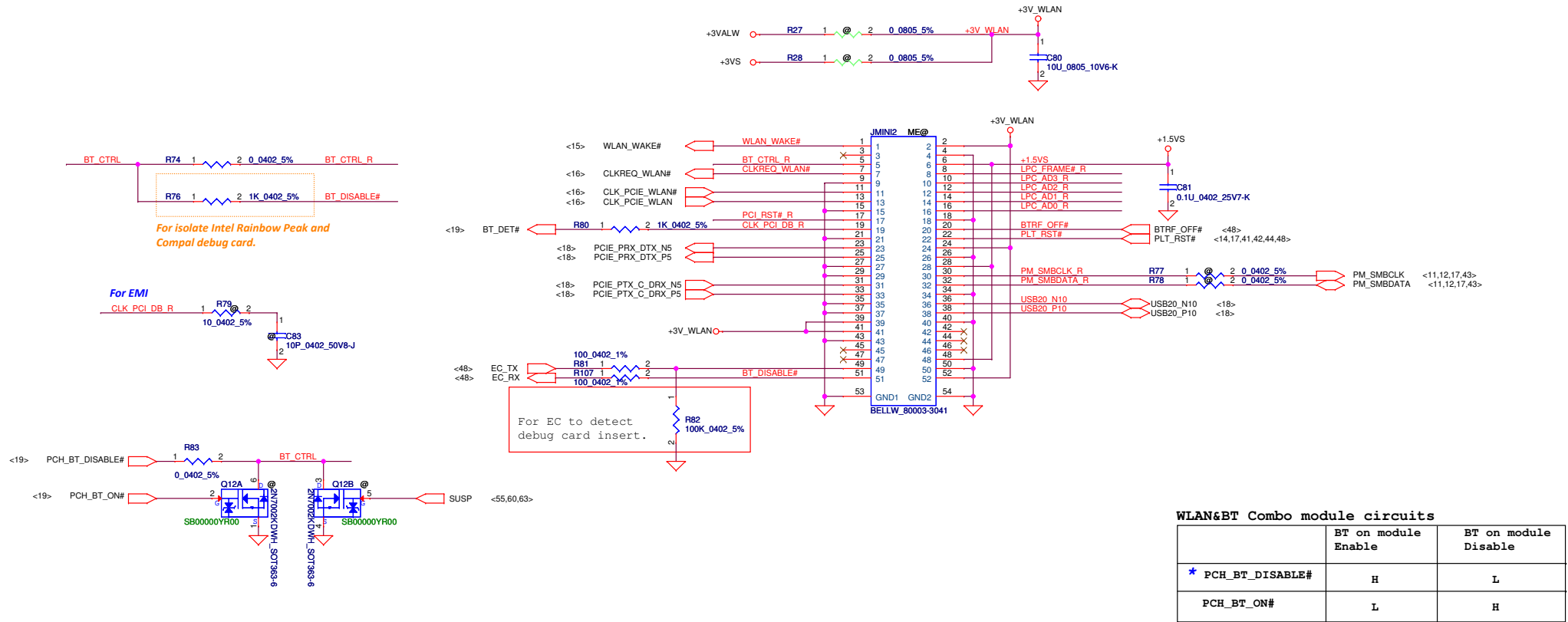


SATA ODD CONN & ODD Power Control

+5VS TO +5VS_ODD



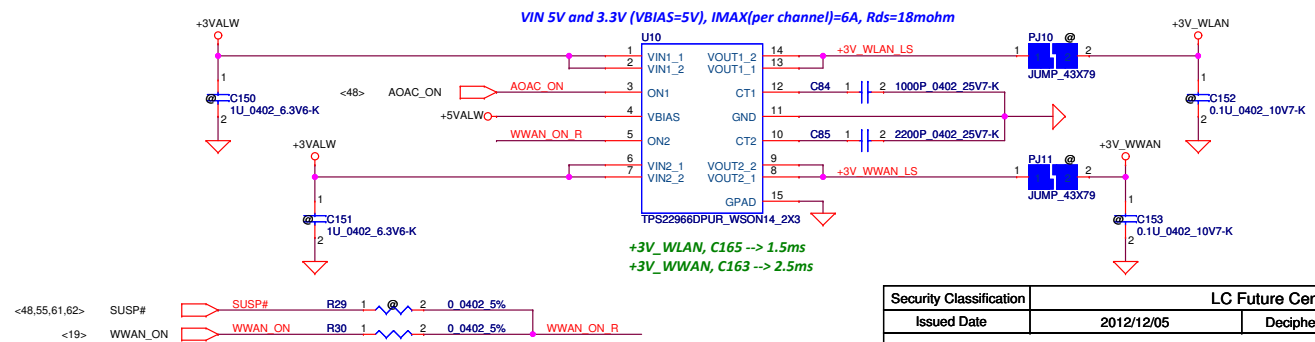
Mini-Express Card(WLAN/WiMAX)



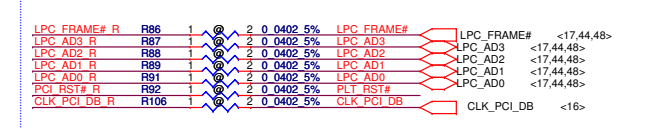
Load Switch

+3VALW To +3V_WLAN
+3VALW To +3V_WWAN

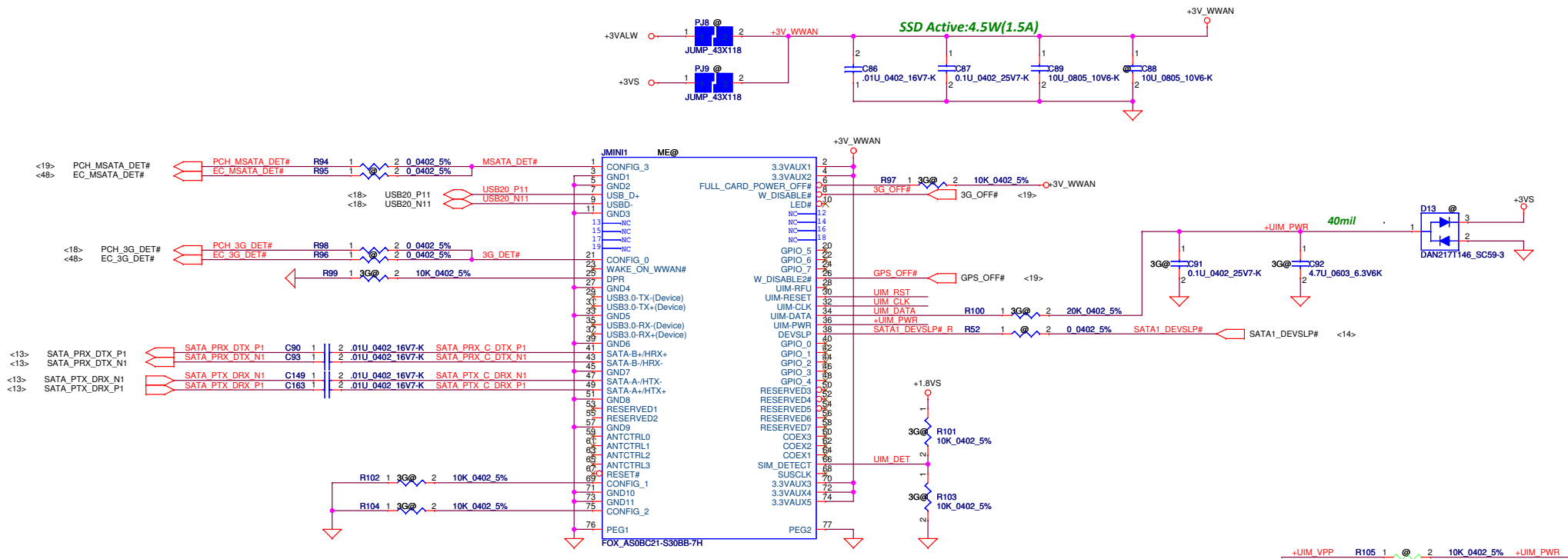
1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
if AOAC disable +3V_WLAN is same as +3VS



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



NGFF(SSD) & SIM CARD CONN.



Only for 15"

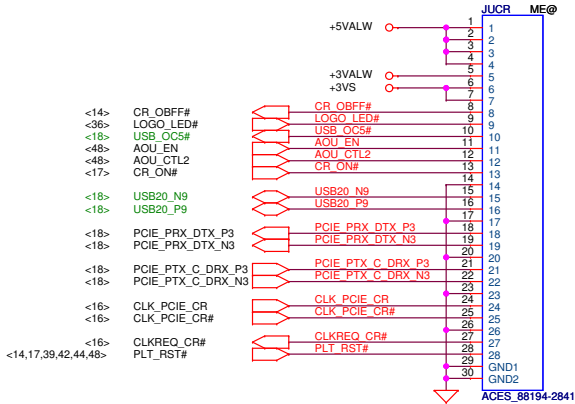
1. PCH_MSATA_DET# --> +3V_PCH
EC_MSATA_DET# --> +3VL
2. PCH_3G_DET# --> +3VS
EC_3G_DET# --> +3VL
需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
a. PCH_3G_DET#
b. PCH_MSATA_DET#

NGFF Detect Desc.

	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0

1.Add CR_WAKE# net for CardReader that
need check with Realtek if need add it and
for what?

USB2.0, CR & LOGO Board

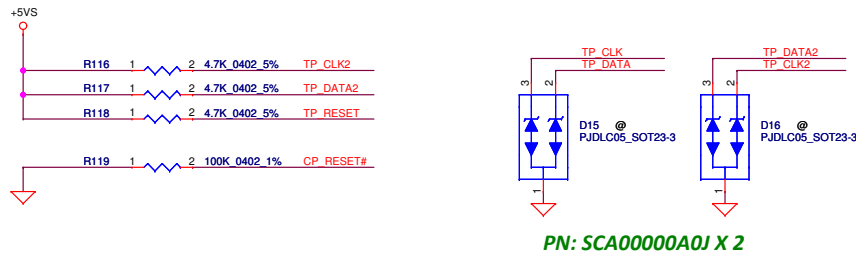
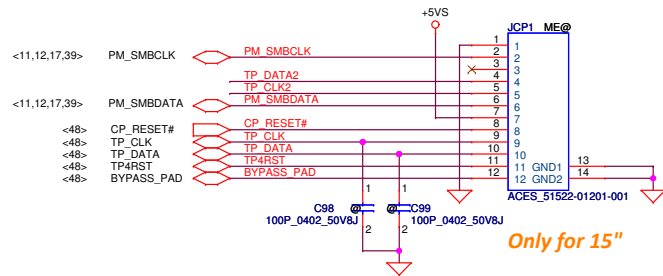


1

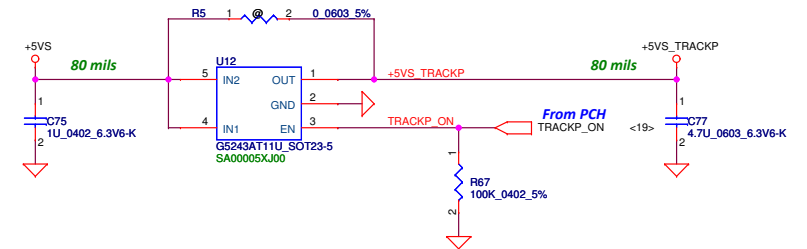
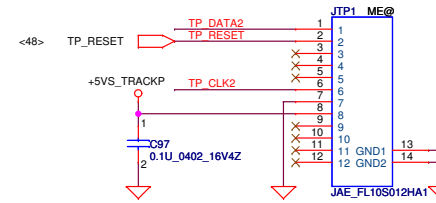


11

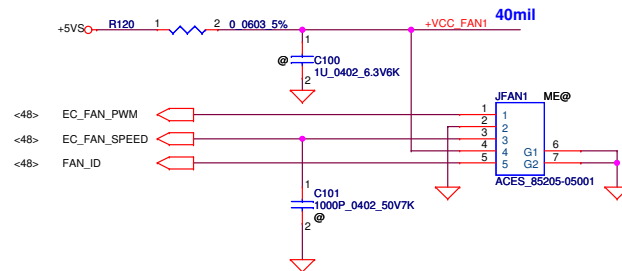
Click Pad



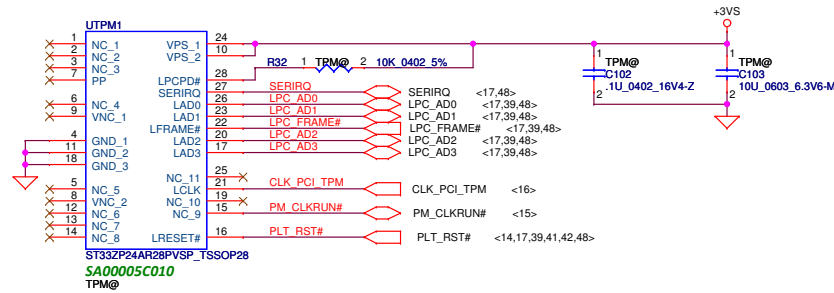
Track point



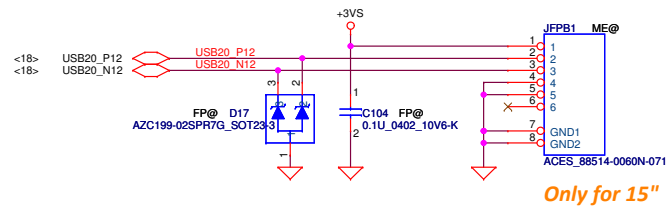
FAN CONN.



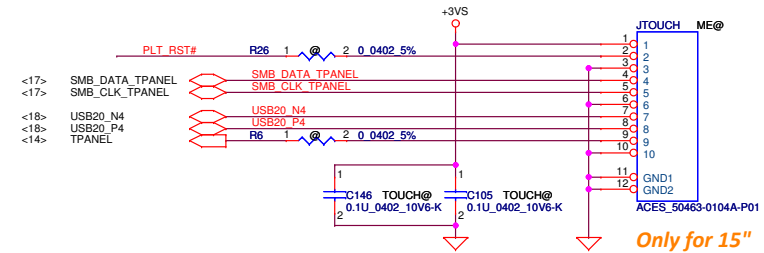
TPM IC



FingerPrint CONN.

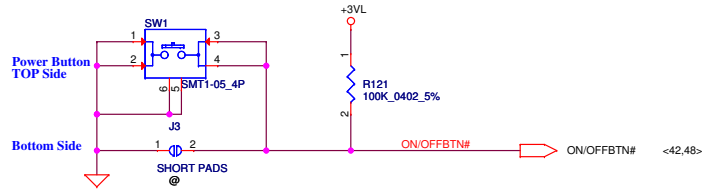


Touch Panel CONN.

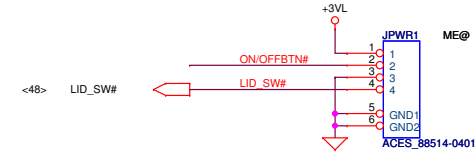


PWR BTN/LID SW CONN.

ON/OFF switch

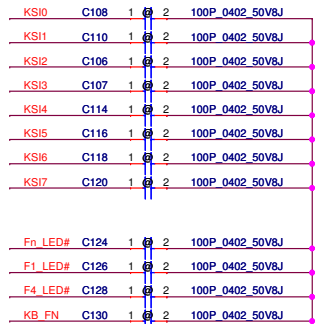


1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

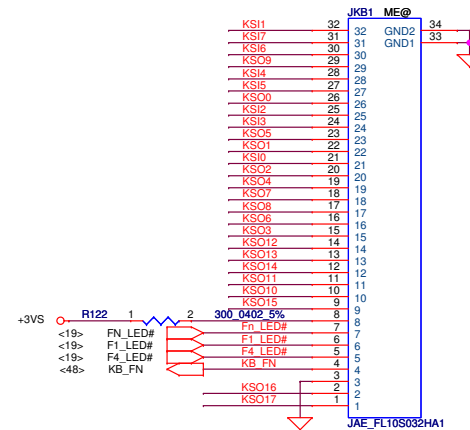
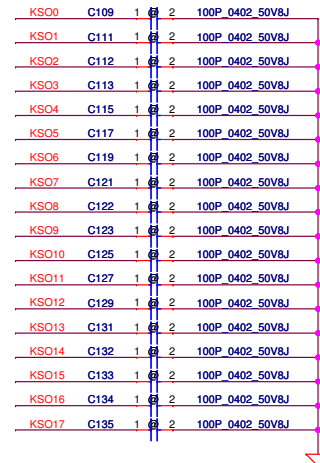


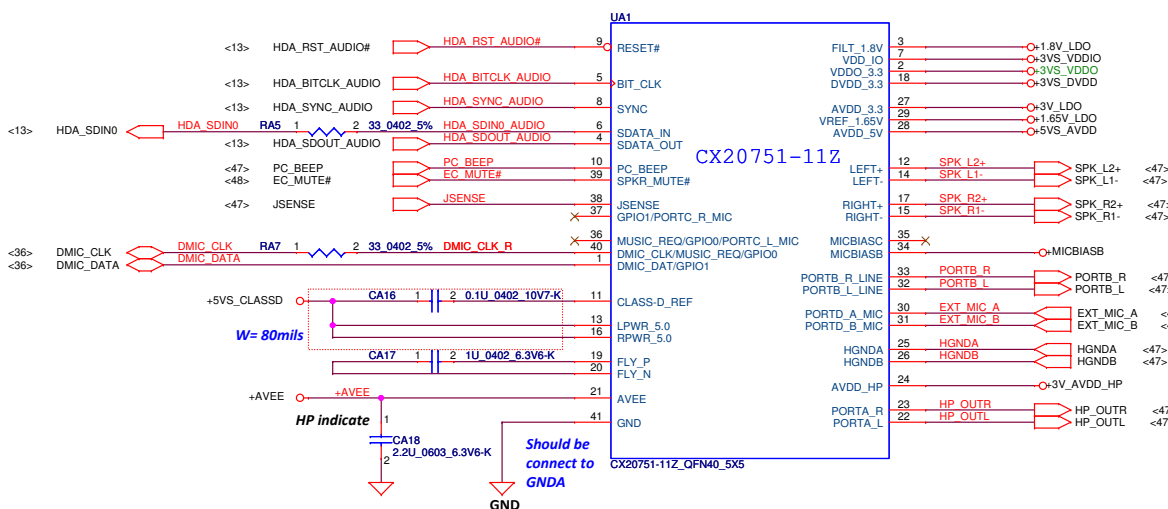
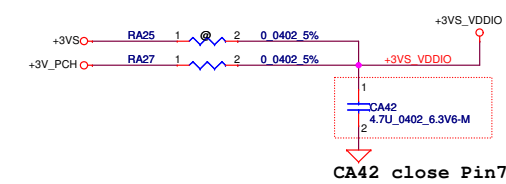
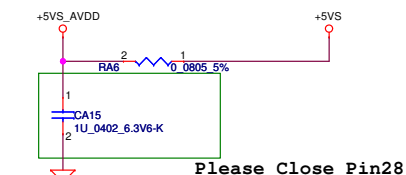
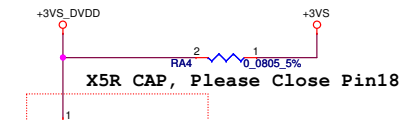
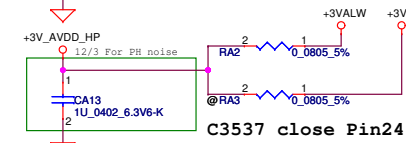
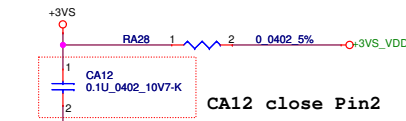
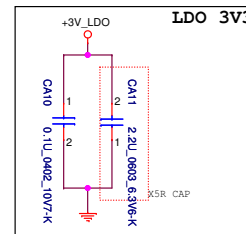
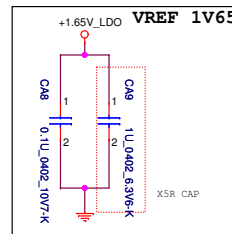
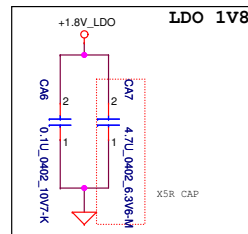
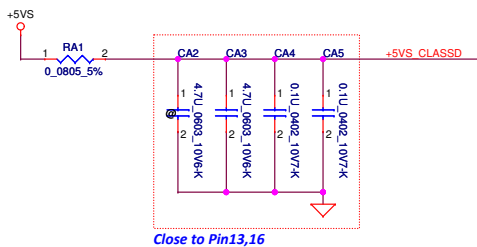
Keyboard CONN.(14")

KSII[0..7] <48>
KSOI[0..17] <48>



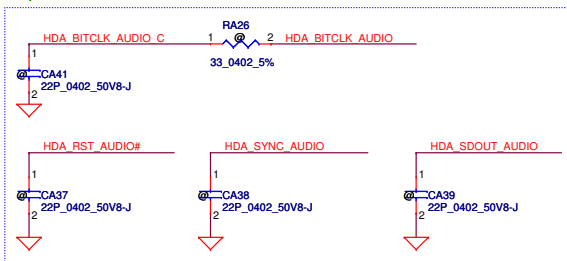
CONN PIN define need double check



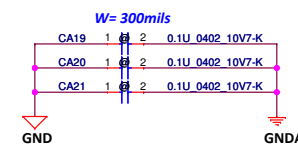
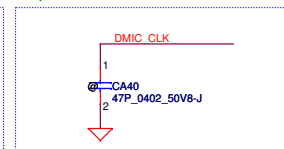


Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A

EMI, close to UA1

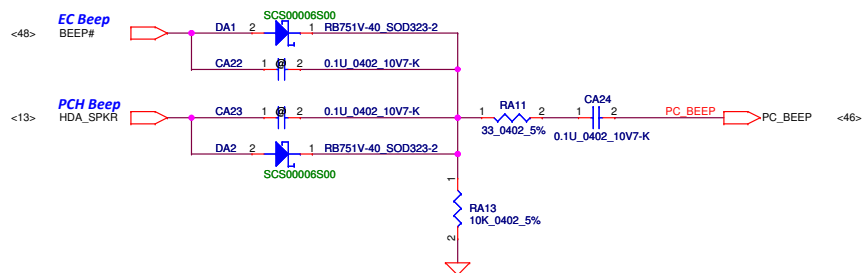


EMI, close to RA7

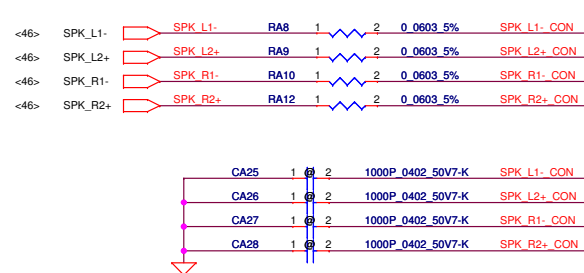


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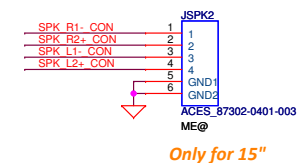
PC Beep



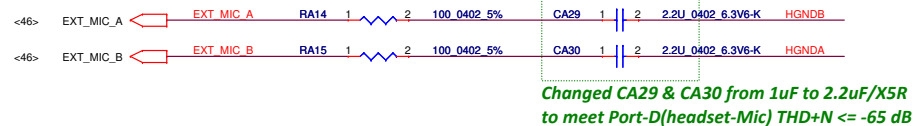
Speaker OUT



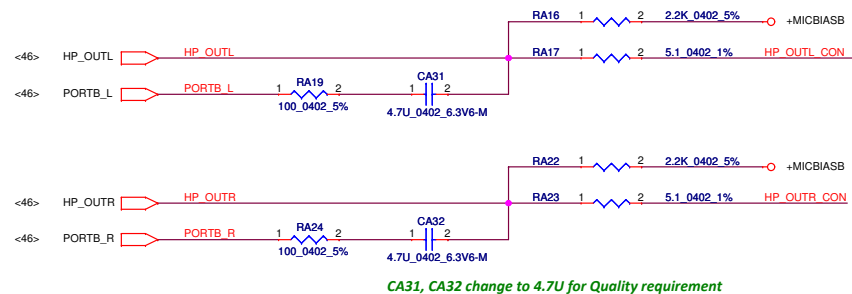
SPK CONN.



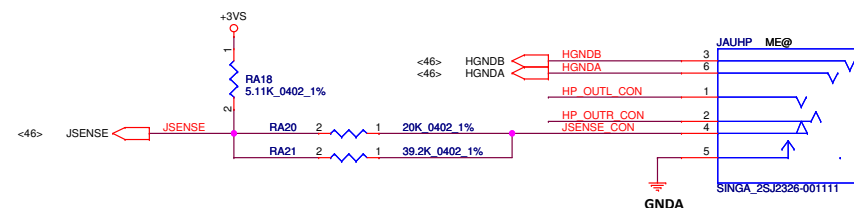
EXT. MIC/LINE IN Apple --> EXT_MIC_A, HGND B
 Nokia --> EXT_MIC_B, HGND A



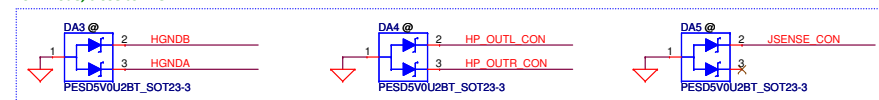
HeadPhone/LINE OUT



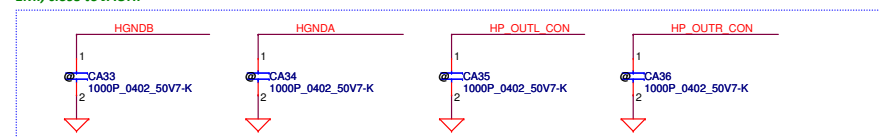
Audio Jack




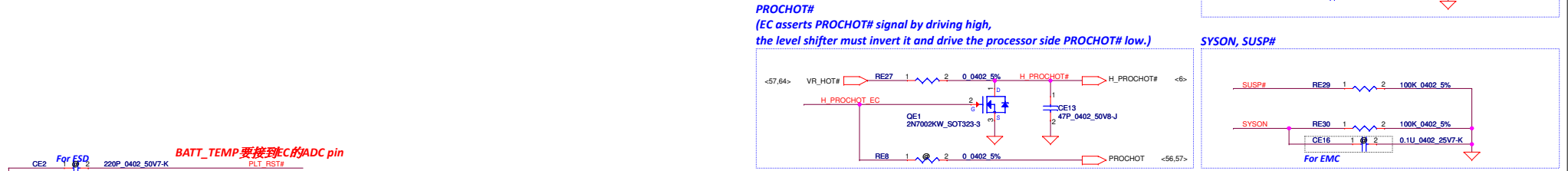
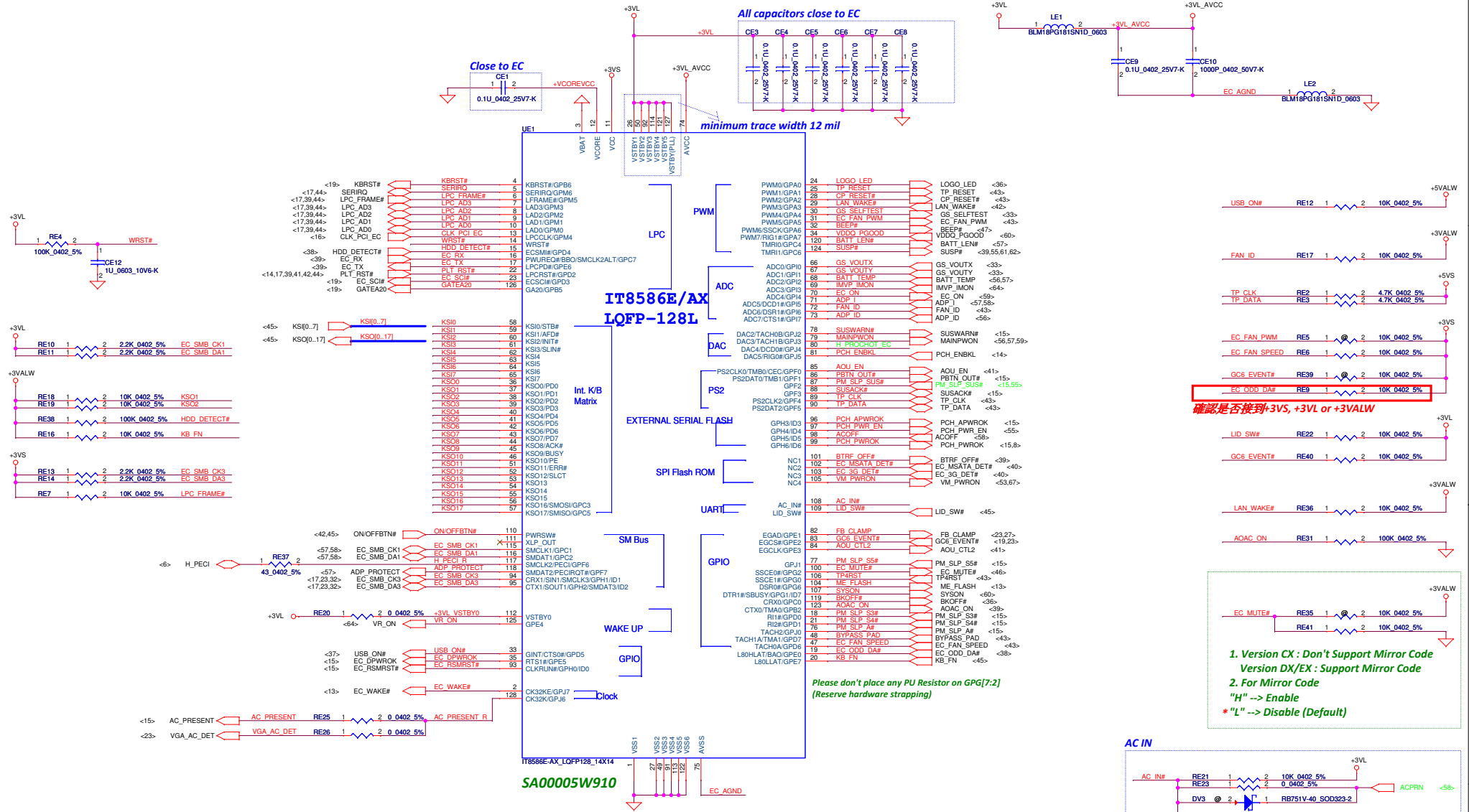
ESD Diode, close to JAUHP

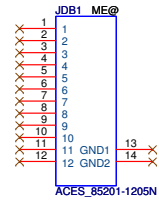


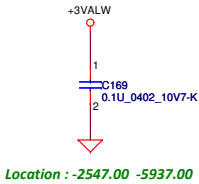
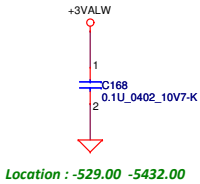
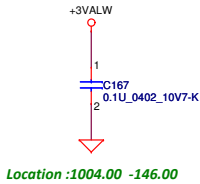
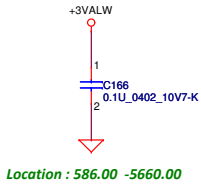
EMI. close to JAUHP

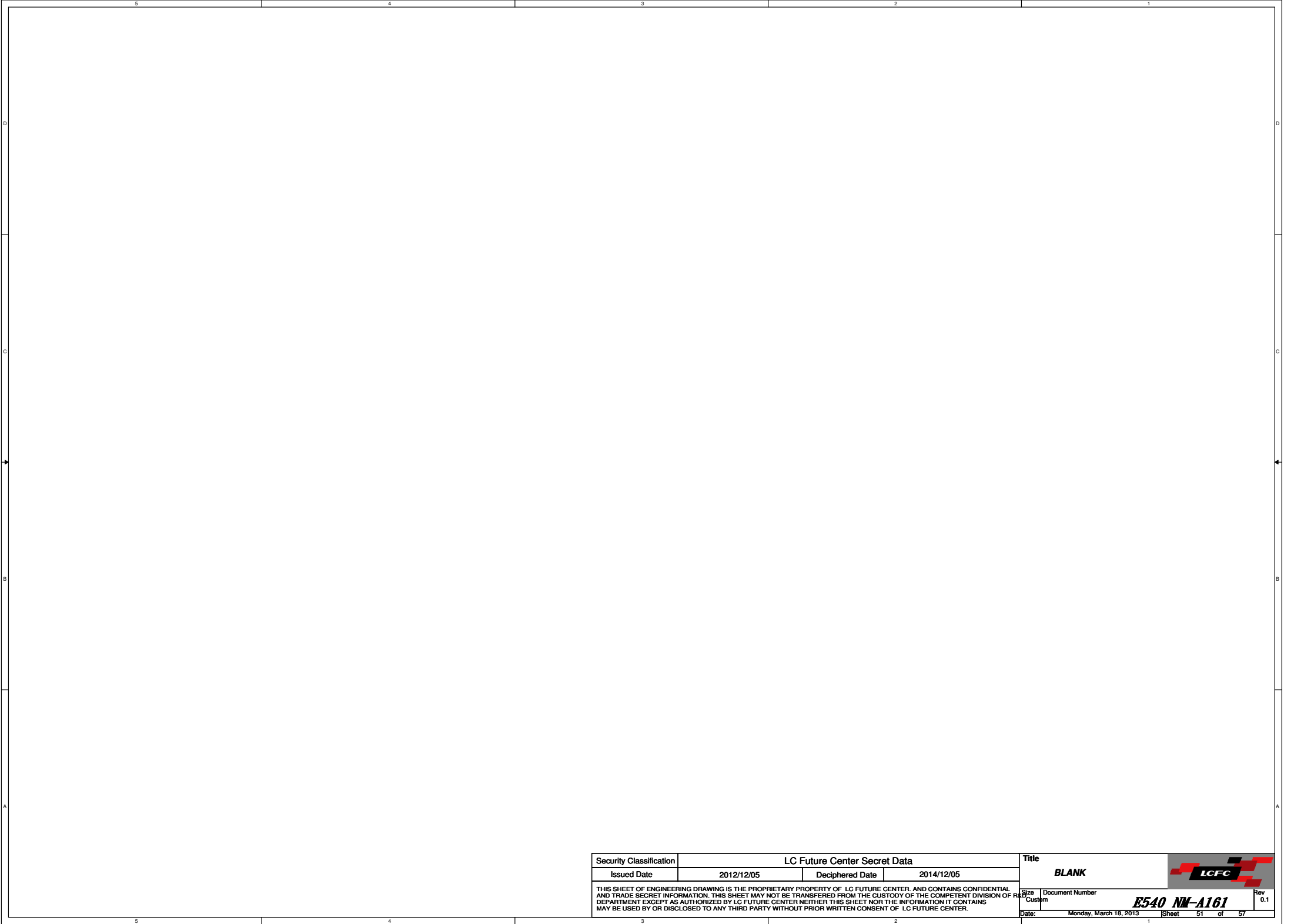



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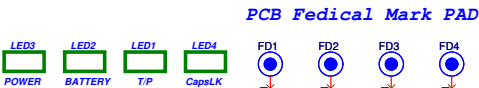
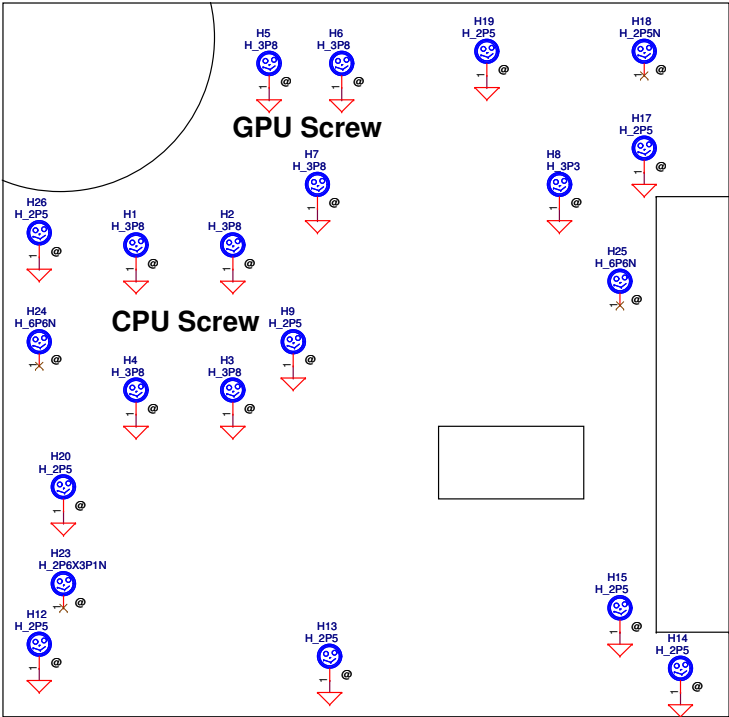






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				Custom		0.1	
				Date:	Monday, March 18, 2013	Sheet	51 of 57
				E540 NW-A161			

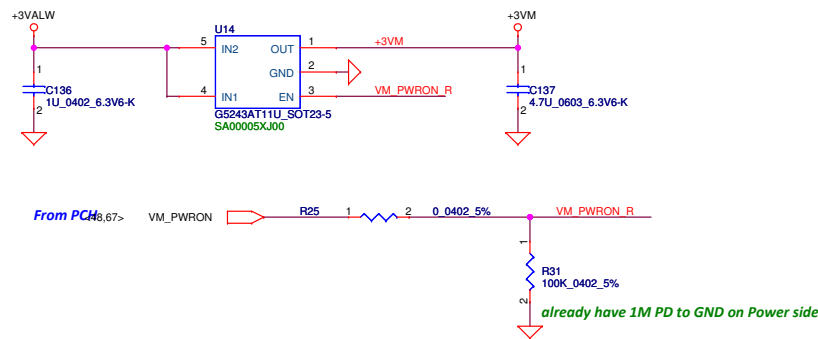
Screw Hole



Security Classification		LC Future Center Secret Data		Title	
Issued Date		2012/12/05		Deciphered Date	
		2014/12/05		2014/12/05	
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Size		Document Number		Rev	
Custom		E540 NM-A161		0.1	
Date:		Monday, March 18, 2013		Sheet 52 of 57	

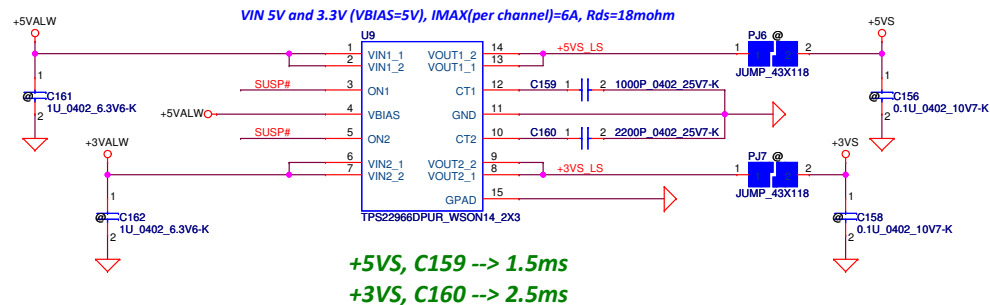
+3VALW to +3VM

FOR SBA Function POWER(always mount)

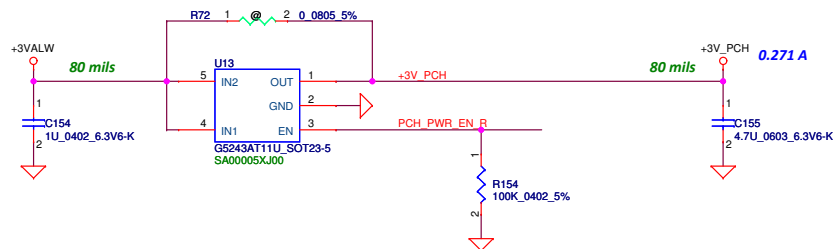
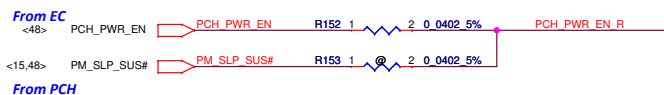


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				Custom	0.1
				Date:	Monday, March 18, 2013
				Sheet	53 of 57

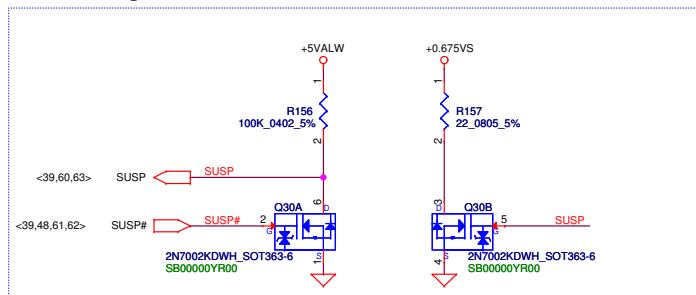
Load Switch
+5VALW To +5VS
+3VALW To +3VS

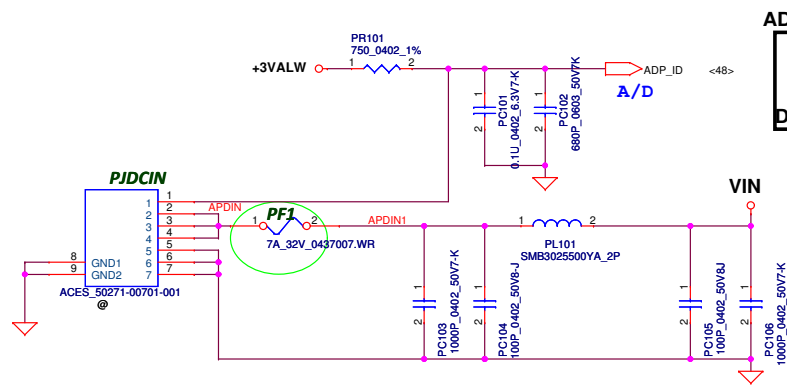


+3VALW To +3V_PCH

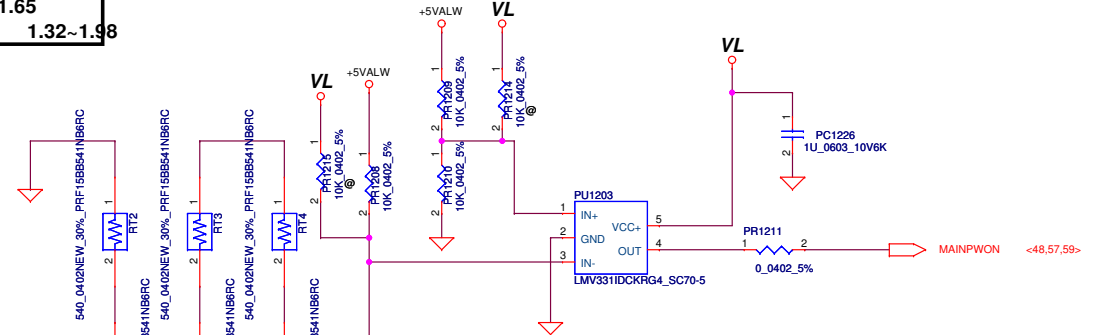


For DisCharge

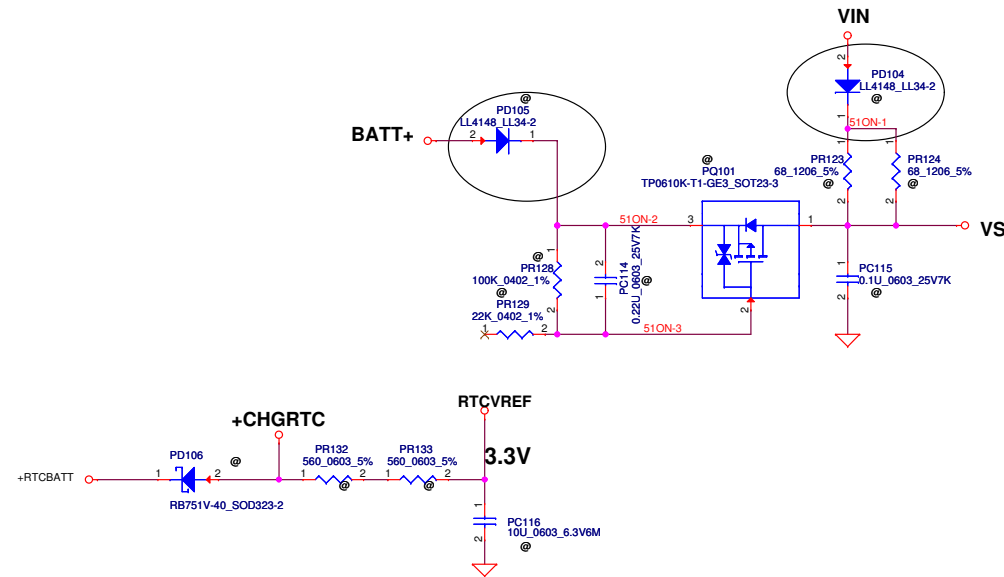




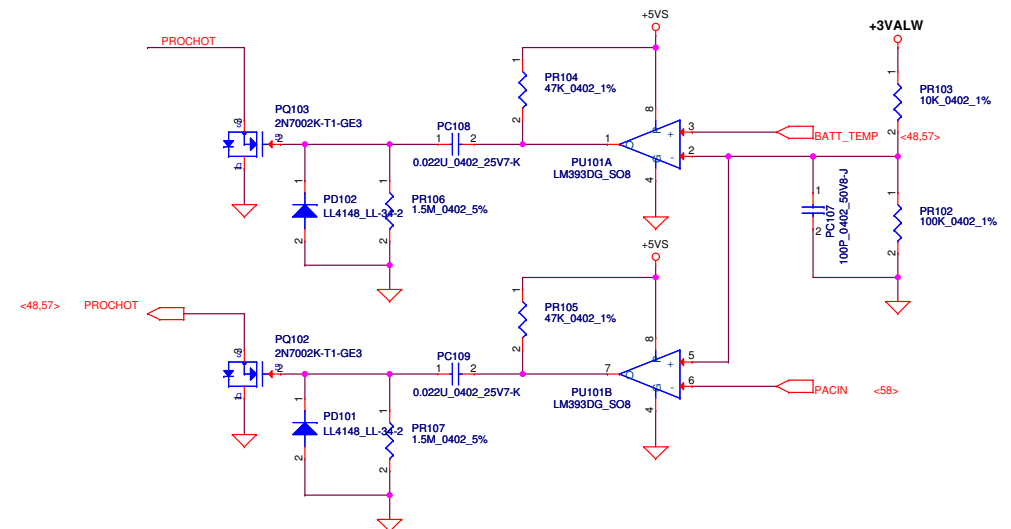
ADP ID			
AC Adapter	90W	65W	
R(K ohm)	open	10	
ADP_ID(V)	3.3	1.65	
Detection voltage	>2.64	1.32~1.98	



Thermal protect
 RT2 place to closed PQ401 with PU401
 RT3 place to closed PQ402 with PU401
 RT4 place to closed PQ501 with PU501
 RT5 place to closed PQ312 with PU301
 RT7 place to closed PQ804 with PU801
 RT8 place to closed PQ1001 with PU901

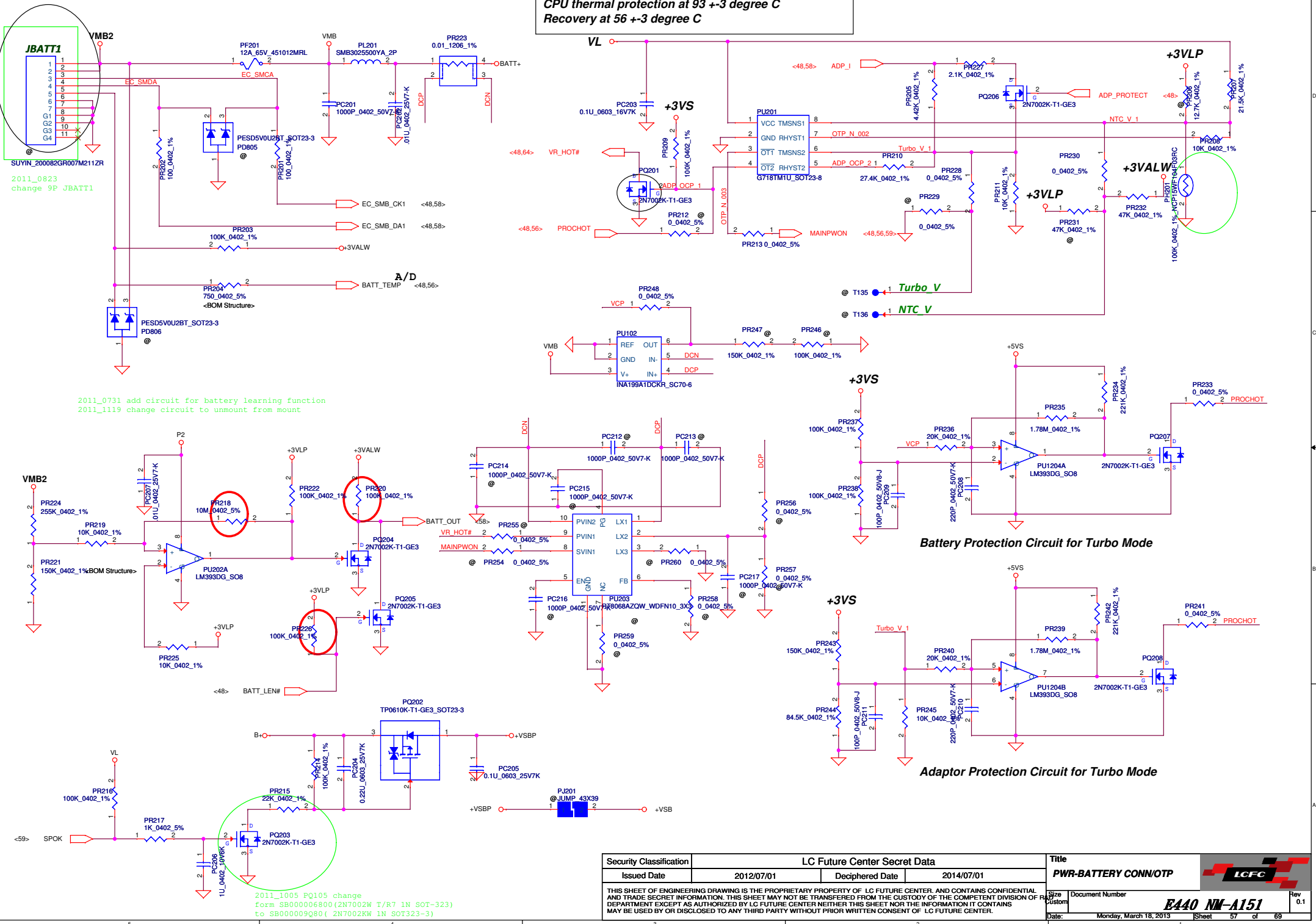


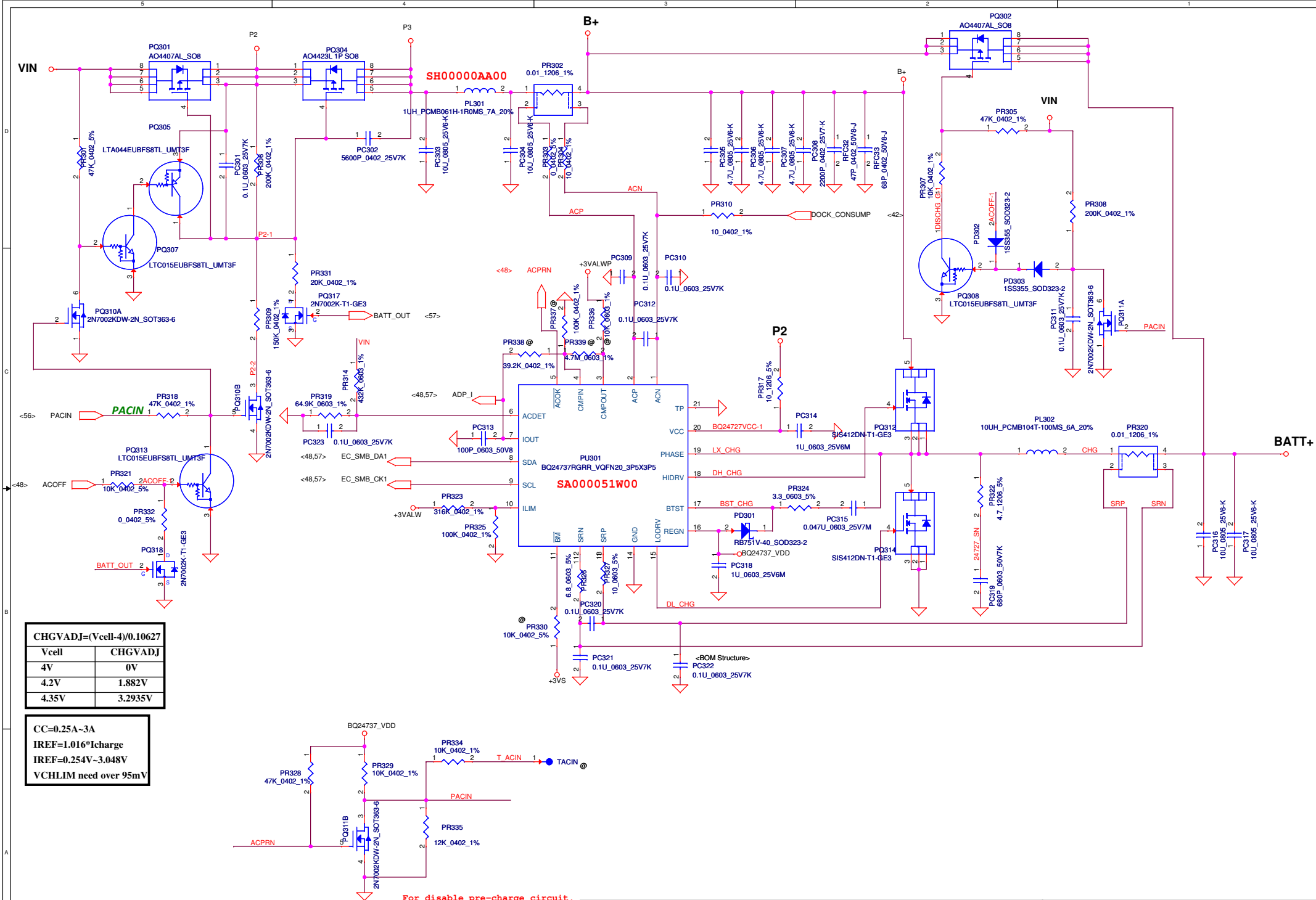
RTC Battery



Security Classification				Title	
LC Future Center Secret Data				PWR-DCIN / Vin Detector	
Issued Date	2012/07/01	Deciphered Date	2014/07/01		
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				Date	Monday, March 18, 2013
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PH1 under CPU bottom side :
CPU thermal protection at 93 ± 3 degree C
Recovery at 56 ± 3 degree C





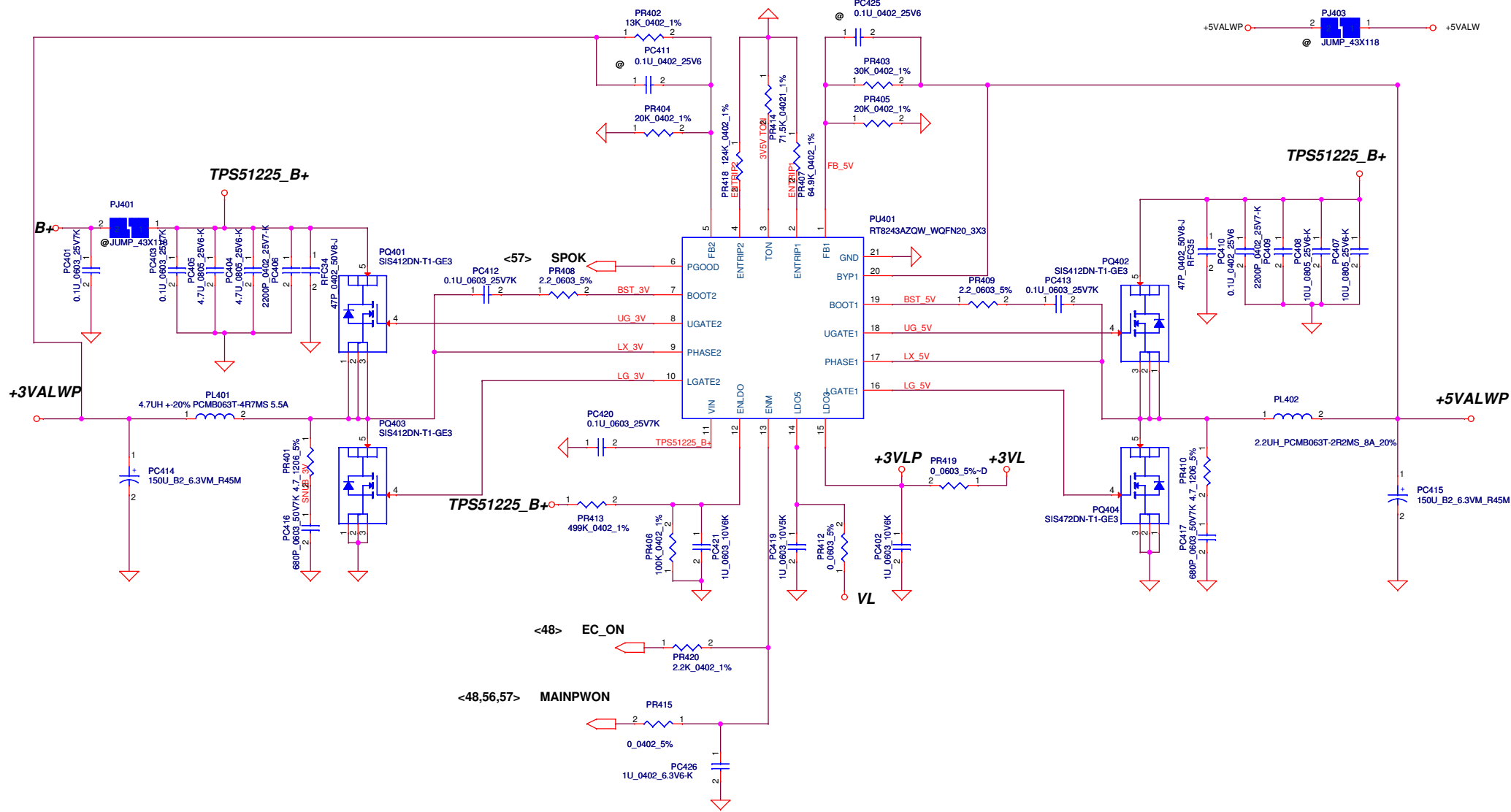
For disable pre-charge circuit.

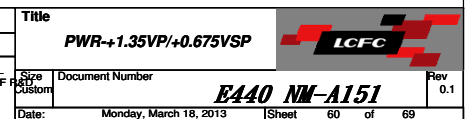
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A	
IREF=1.016*Icharge	
IREF=0.254V~3.048V	
VCHLIM need over 95mV	

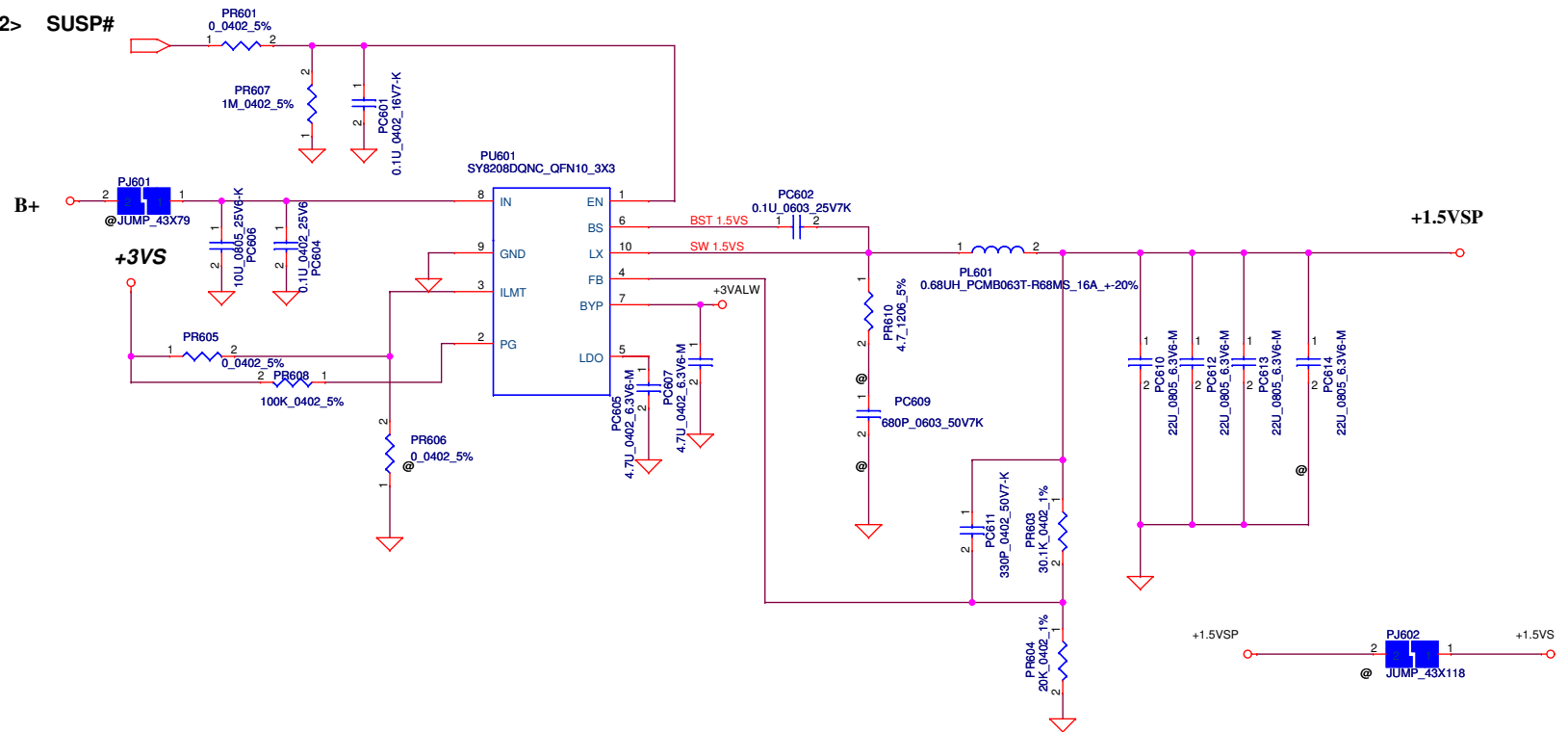
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LC Future Center Secret Data			
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PWR-CHARGER-BQ24737			
Size	Document Number	E440 NW-A151	
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<39,48,55,62> SUSP#

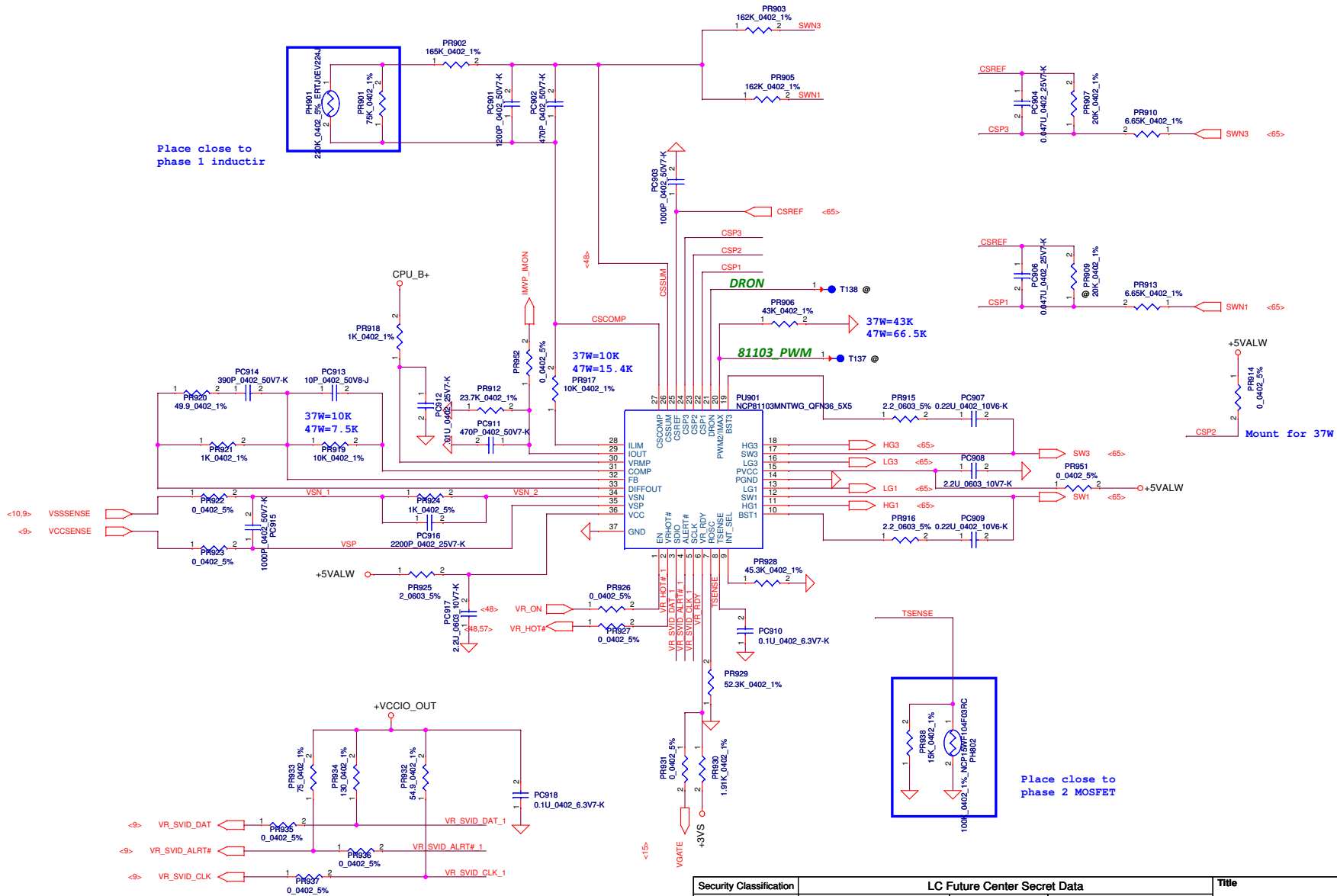


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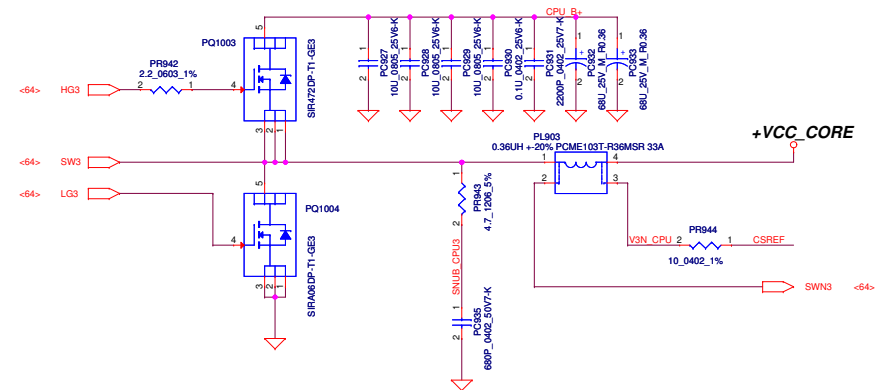
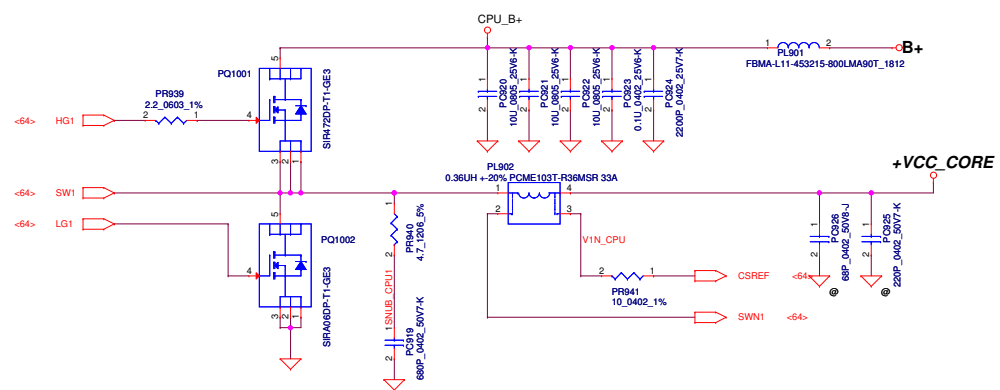
Title		LCFC	
PWR-+1.5VSP			
Size	Document Number	E440 NM-A151	
Custom			
Date:	Monday, March 18, 2013	Sheet	61 of 69

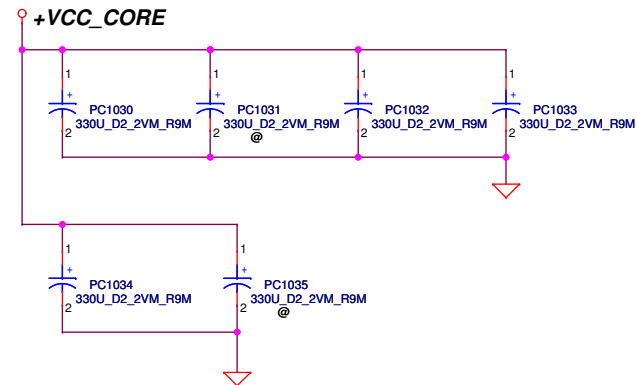
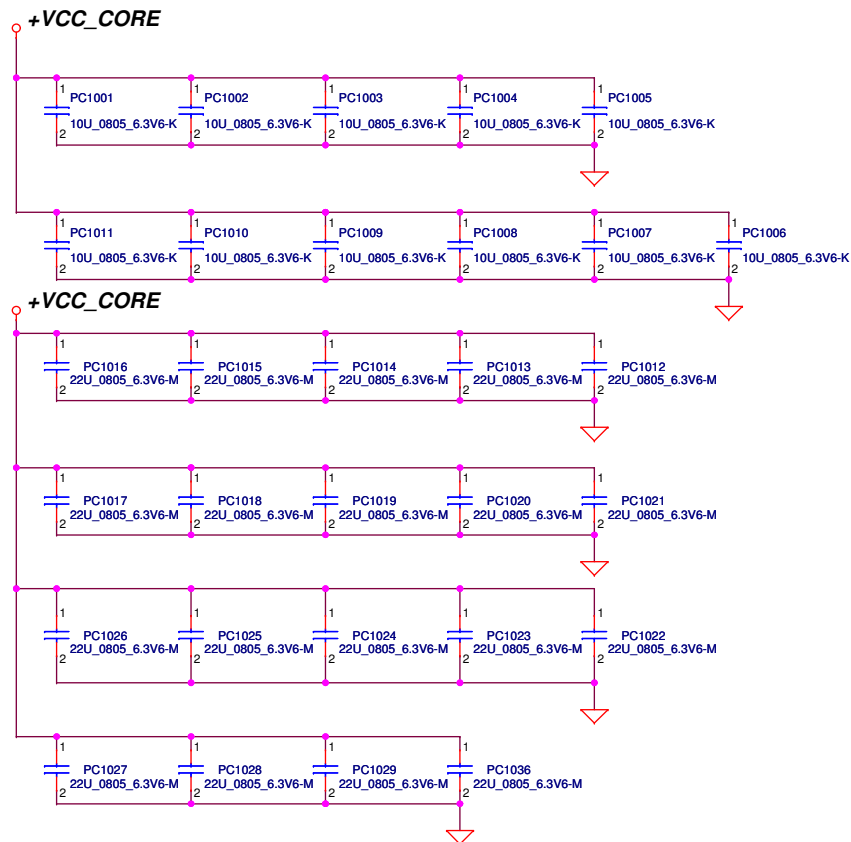
Place close to
phase 1 inductor


Place close to
phase 2 MOSFET

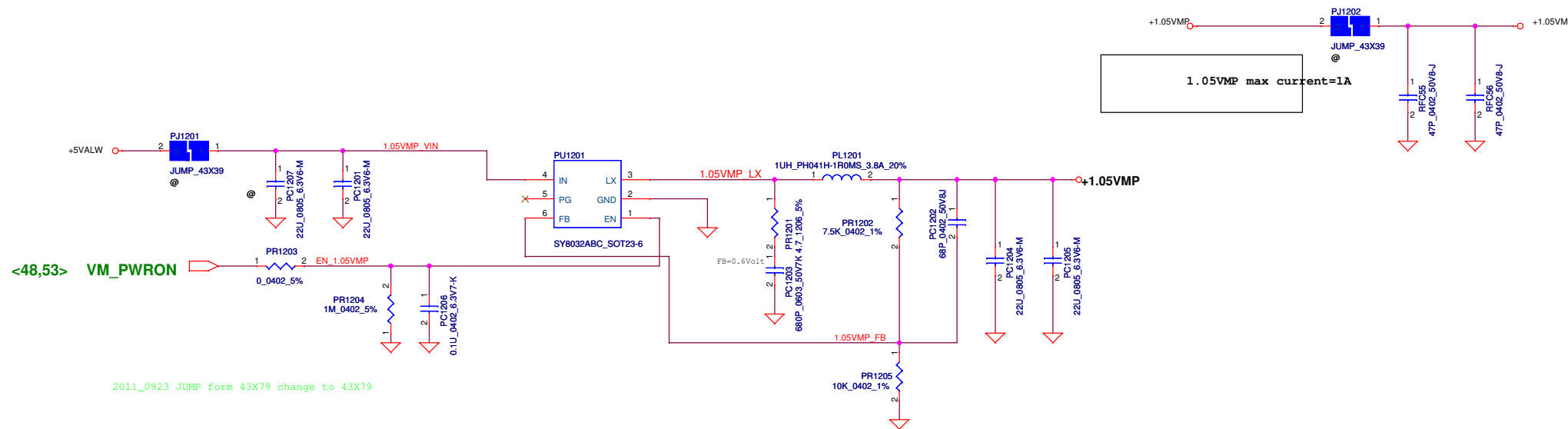




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				Custom			
				Date:	Monday, March 18, 2013	Sheet	66 of 69

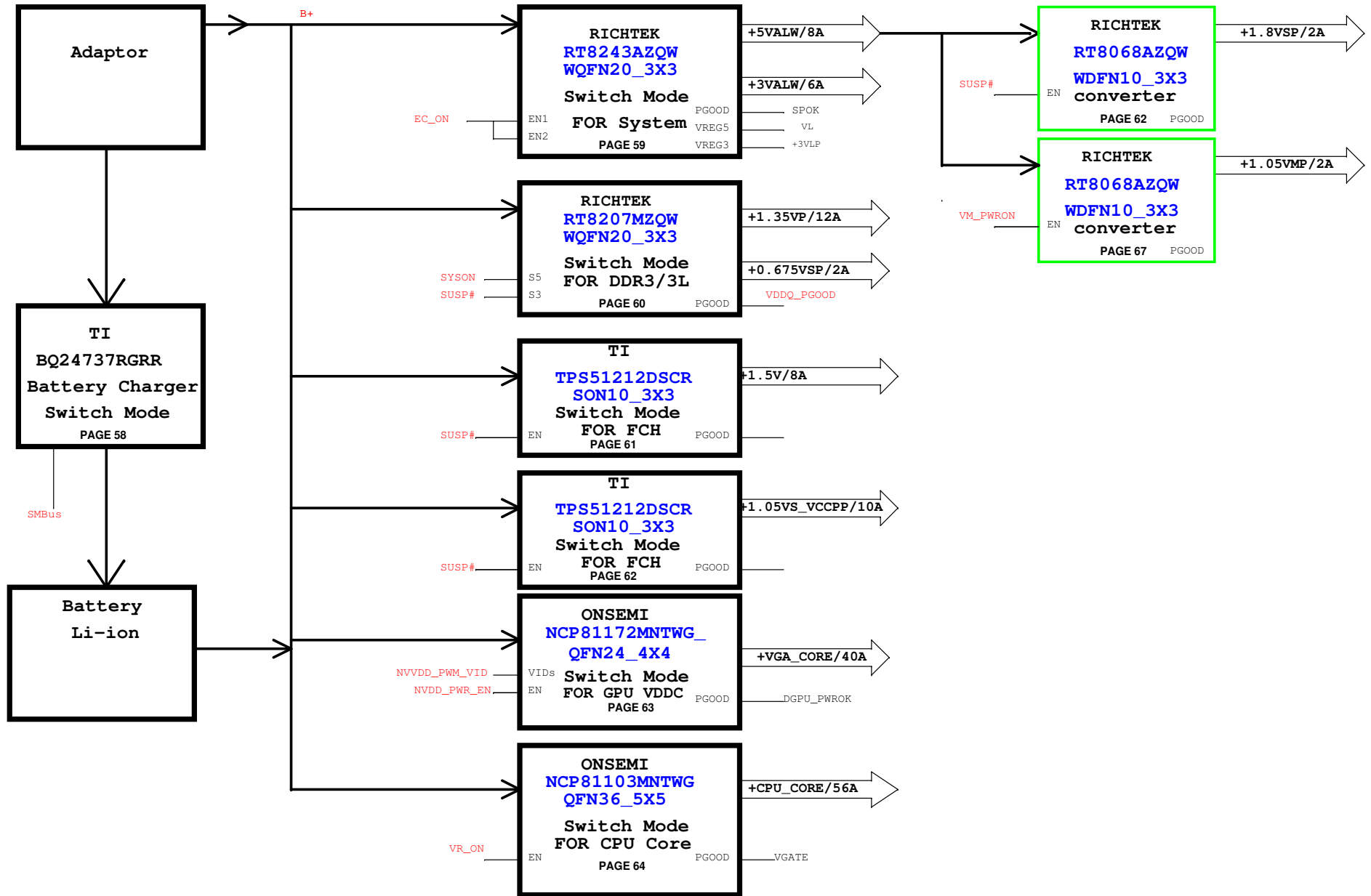


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Issued Date		2012/07/01		Deciphered Date		2014/07/01				PWR-+1.05VMP	
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POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE



HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"
				For Deep S3 Function

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Title	
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				Rev 0.1	
Date: Monday, March 18, 2013				Sheet 69 of 69	